

P-Ch 40V Fast Switching MOSFETs

Features:

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Description:

The KNS4101 is the high cell density trench P-ch MOSFETs, which provides excellent $R_{DS(on)}$ and efficiency for most of the small power switching and load switch applications.

The KNS4101 meet the RoHS and Green Product requirement with full function reliability approved.

Product Summary

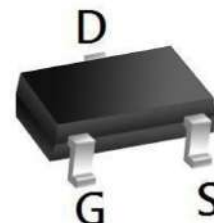
BVDSS	$R_{DS(on)}$	I_D
-40V	70m Ω	-3.2A

Absolute Maximum Ratings

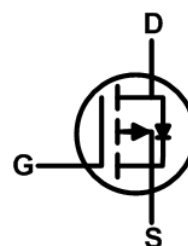
Symbol	Parameter	Rating		Units
		10s	Steady State	
V_{DS}	Drain-Source Voltage	-40		V
V_{GS}	Gate-Source Voltage	± 20		V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -4.5V ¹	-3.7	-3.2	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -4.5V ¹	-3.0	-2.6	A
I_{DM}	Pulsed Drain Current ²	-16.1		A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ³	1.32	1	W
$P_D@T_A=70^\circ\text{C}$	Total Power Dissipation ³	0.84	0.64	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	125	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤ 10 s)	---	95	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	80	$^\circ\text{C/W}$



SOT 23 Pin Configuration



Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.018	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5V, I_D=-3A$	---	---	70	$m\Omega$
		$V_{GS}=-2.5V, I_D=-2A$	---	---	100	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	---	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.5	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-3A$	---	5.8	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-32V, V_{GS}=-4.5V, I_D=-3A$	---	6.4	---	nC
Q_{gs}	Gate-Source Charge		---	2.1	---	
Q_{gd}	Gate-Drain Charge		---	2.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-20V, V_{GS}=-4.5V, R_G=3.3\Omega, I_D=-3A$	---	4.2	---	ns
T_r	Rise Time		---	23	---	
$T_{d(off)}$	Turn-Off Delay Time		---	26.8	---	
T_f	Fall Time		---	20.6	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	620	---	pF
C_{oss}	Output Capacitance		---	65	---	
C_{rss}	Reverse Transfer Capacitance		---	53	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-3.2	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-16.1	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3. The power dissipation is limited by 150°C junction temperature

4. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

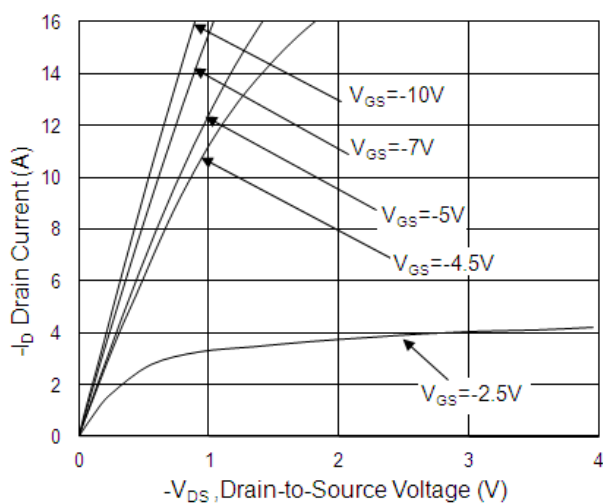


Fig.1 Typical Output Characteristics

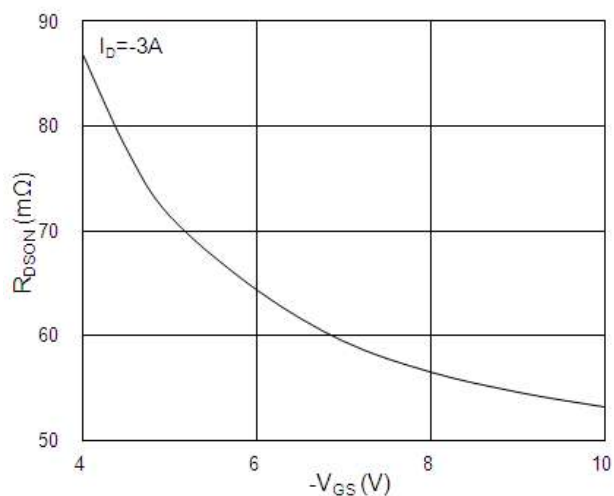


Fig.2 On-Resistance vs. G-S Voltage

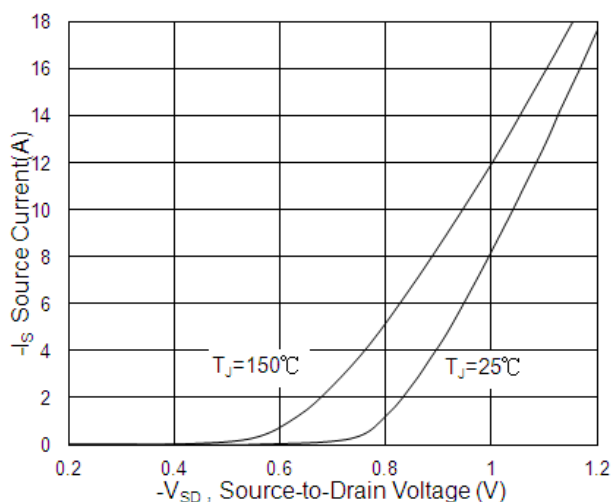


Fig.3 Forward Characteristics Of Reverse

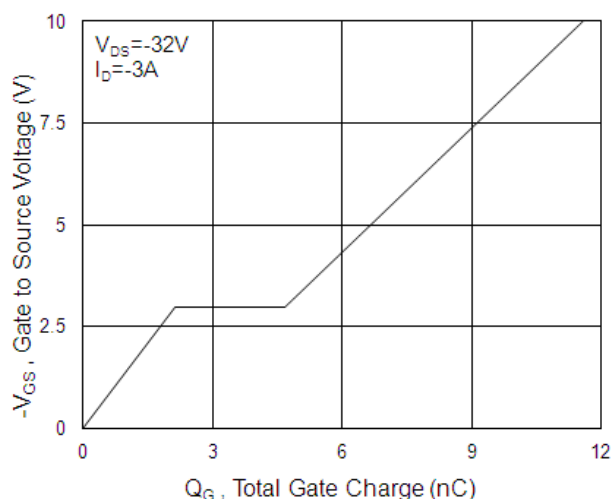


Fig.4 Gate-Charge Characteristics

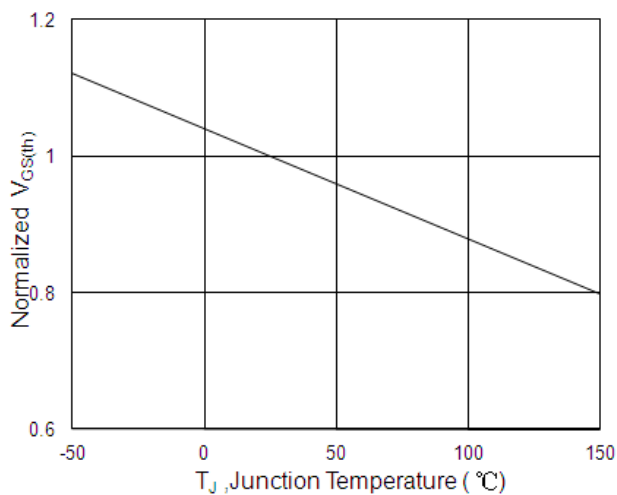


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

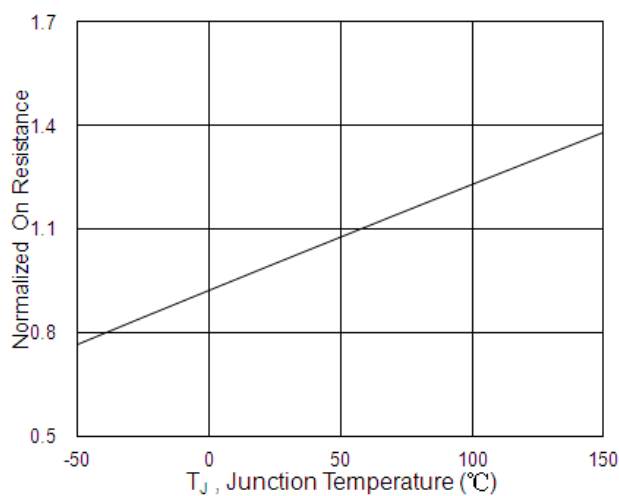


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

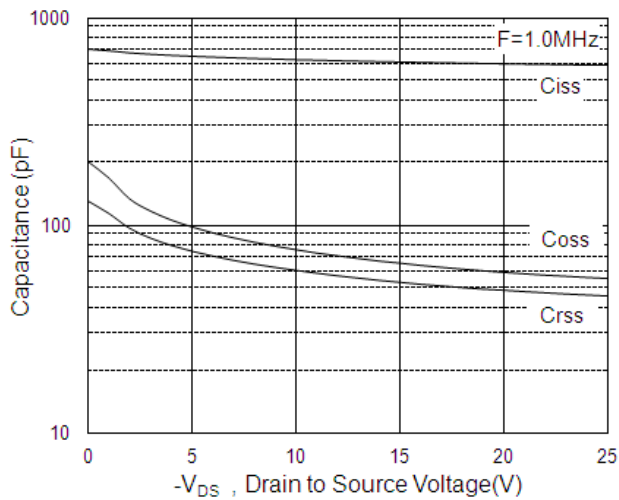


Fig.7 Capacitance

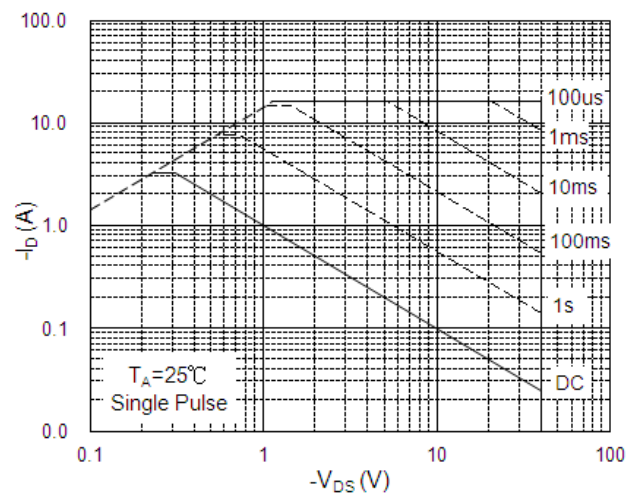


Fig.8 Safe Operating Area

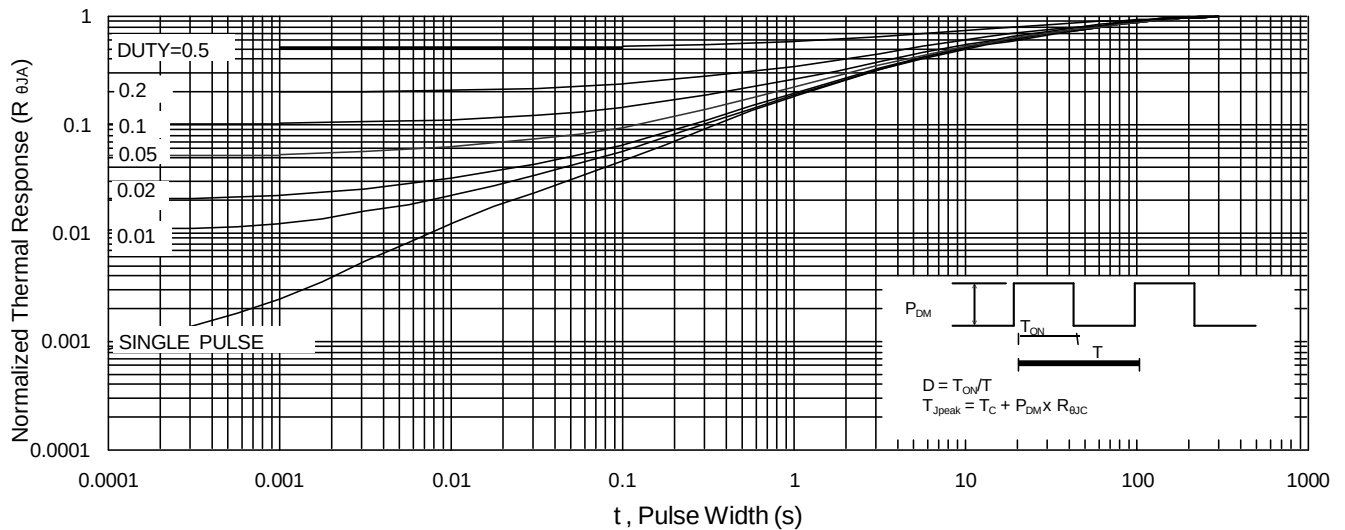


Fig.9 Normalized Maximum Transient Thermal Impedance

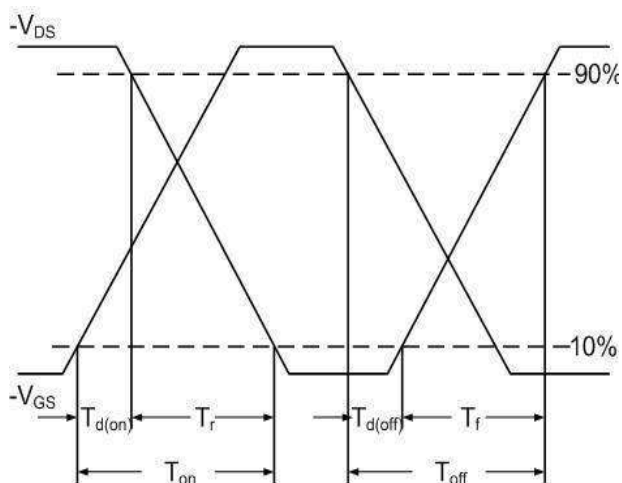


Fig.10 Switching Time Waveform

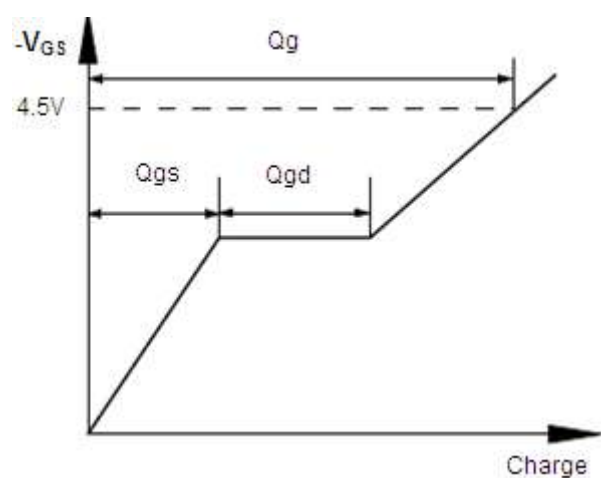
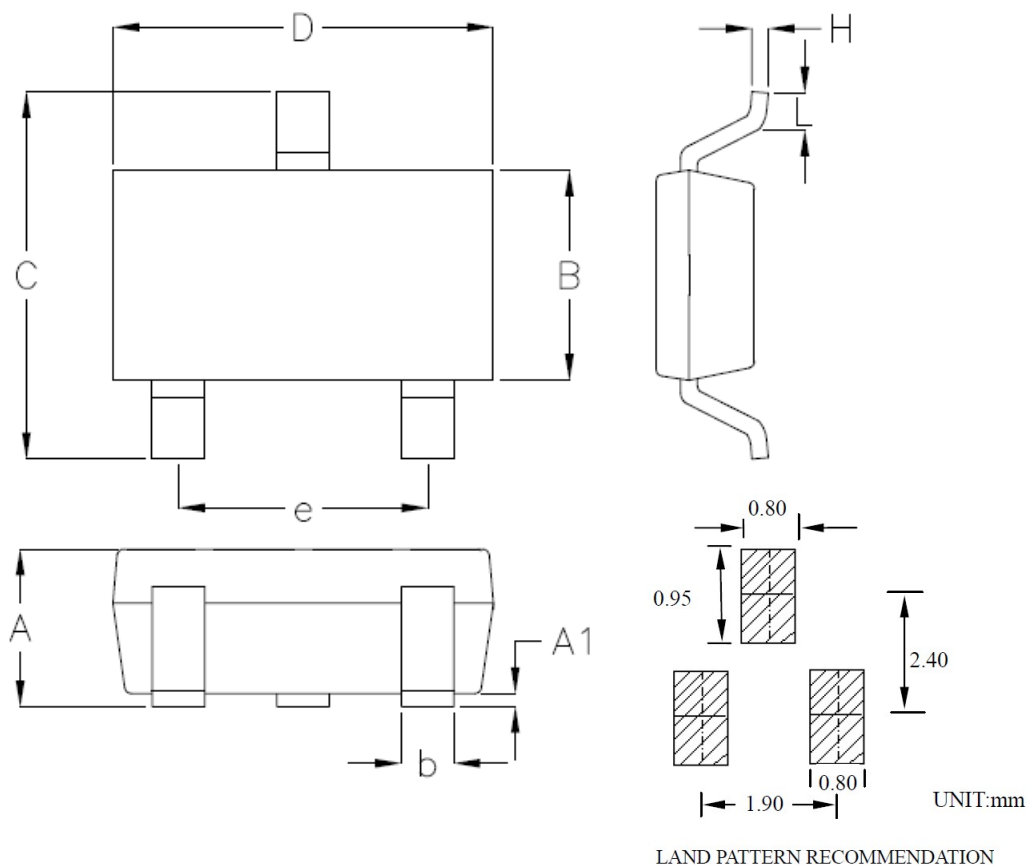


Fig.11 Gate Charge Waveform

SOT-23 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.890	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.508	0.014	0.020
C	2.591	3.010	0.102	0.119
D	2.692	3.099	0.106	0.122
e	1.793	2.007	0.070	0.079
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

Marking:

