650V N-Channel Super Junction Power MOSFET

Description:

This series of power MOSFET use N channel Multi-EPI Super-Junction technology and design to provide better characteristics, such as fast switching time, low Ciss and Crss, low on resistance and excellent avalanche characteristics,making it especially suitable for applications which require superior power density and outstanding efficiency.

Product Summary			
V_{DS}	$R_{DS(on)}$(mΩ)Typ	I_D(A)	Qg(Typ)
650V	35 @ 10V,35A	77	300nc

Features:

- Low on-resistance
- Ultra low gate charge and input capacitance
- 100% avalanche tested
- Rohs compliant

TO-3P
KWSJ77N65KR

TO-247
KWSJ77N65PR

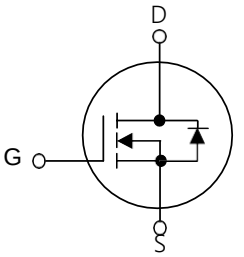
Mechanical Data:

- Case:TO-247,TO-3P Package

Application:

- Switching applications
- SMPS
- UPS
- Solar
- Lighting

Block Diagram



Pin Definition:

1. Gate
2. Drain
3. Source

Ordering Information

Part No.	Package Type	Package	Quality(box)
KWSJ77N65PR	TO-247	Tube	600
KWSJ77N65KR	TO-3P	Tube	600

Table1 Absolute Maximum Ratings (T_C=25℃, unless otherwise specified)

Parameters		Symbol	KWSJ77N65PR KWSJ77N65KR	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Contionous Drain Current	T_C=25°C	I_D	77	A
	T_C=100°C		45	
Pulsed Drain Current (Note 1)		I_{DM}	260	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	1950	mJ
Avalanche Current(Note 1)		I_{AR}	13	A
Repetitive Avalanche Energy(Note 1)		E_{AR}	2.5	mJ
Reverse Diode Recovery dv/dt(Note 3)		dv/dt	15	V/ns
Drain Source Voltage Slope (V_{DS}=480V)		dv/dt	50	V/ns
Power Dissipation T_C=25°C		P_D	400	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55 ~ +150	℃

Table 2.Thermal Characteristics

Parameters	Symbol	KWSJ77N65KR / KWSJ77N65PR	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	62	℃/W
Thermal resistance Junction to Case	$R_{\theta JC}$	0.32	℃/W

Table 3. Electrical Chatacteristics (T_J=25℃, unless otherwise specified)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	650			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=650V,V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V			100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V			-100	nA
On Characteristics(Note 4)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=35A		35	41	mΩ
Dynamic Characteristics(Note 5)							
Input Capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1MHz		6200		pF
Output Capacitance		C_{OSS}			300		pF
Reverse Transfer Capacitance		C_{RSS}			12		pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V_{DD}=520V,I_D=35A, V_{GS}=10V,R_G=20Ω		39		ns
Turn-On Rise Time		tr			20		ns
Turn-Off Delay Time		td(off)			100		ns
Turn-Off Fall Time		tf			5		ns
Total Gate Charge		Q_G	V_{DS}=520V,I_D=35A, V_{GS}=10V		300		nC
Gate-Source Charge		Q_{GS}			59		nC
Gate-Drain Charge		Q_{GD}			195		nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V,I_S=35A		0.9	1.5	V
Maximum Continuous Drain-Source Diode Forward Current(Note 4)		I_S				77	A
Reverse Recovery Time		trr	V_{GS}=0V,I_S=35A dI$_F$/dt=100A/μs(Note 4)		290		ns
Reverse Recovery Charge		Q_{RR}			12		μC

Notes：1 Repetitive Rating:Pulse width limited by maximum junction temperature 2
Pulse width tp limited by Tj,max
3 V_{DD}≤BV_{DSS},starting T_J=25℃
4 Pulse Test: Pulse width ≤300μS,Duty cycle≤2%5
Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

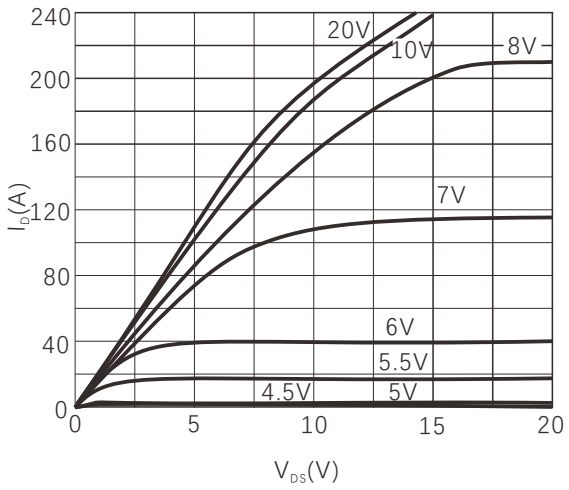


Figure 2. Transfer Characteristics

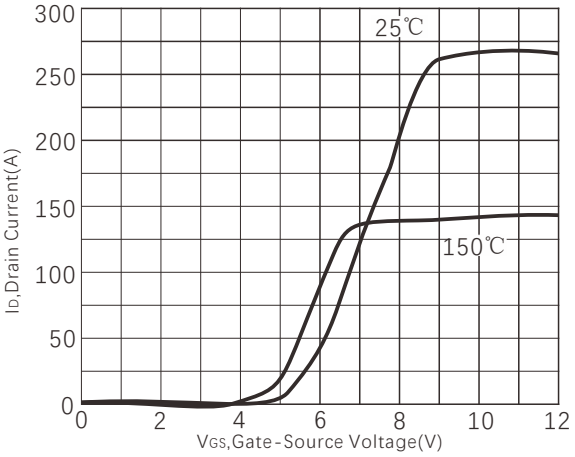


Figure 3.On-Resistance vs.Drain Current

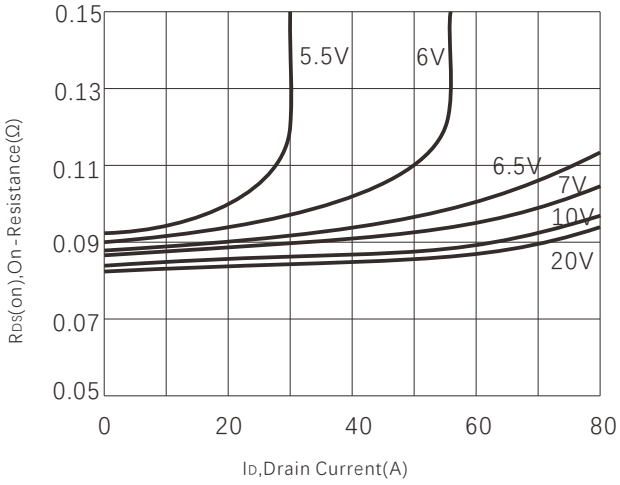


Figure 4. Capacitance

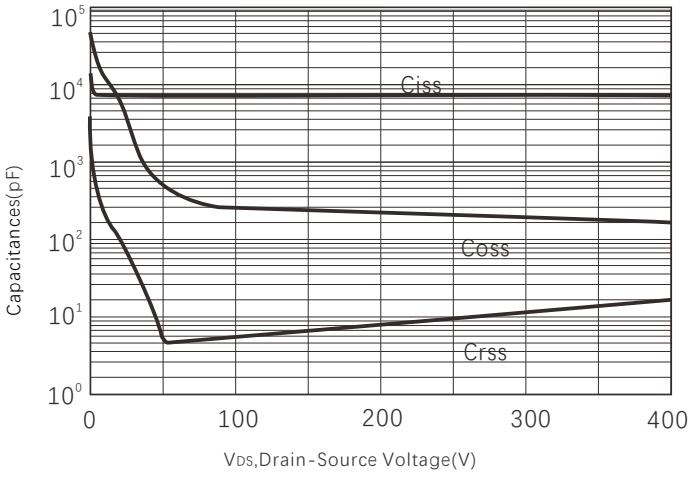


Figure 5.Gate charge

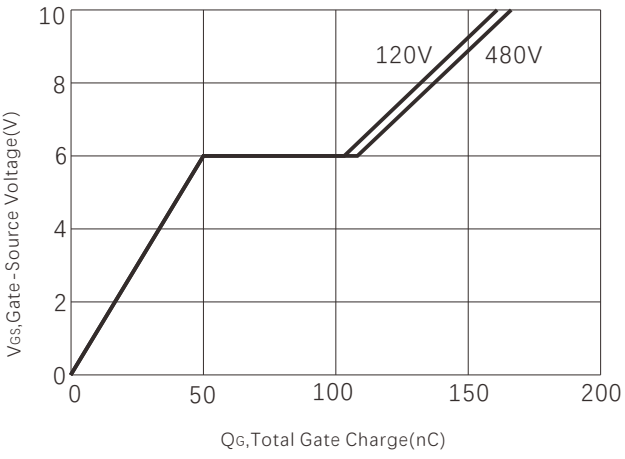


Figure 6.Source-Drain Diode Forward Voltage

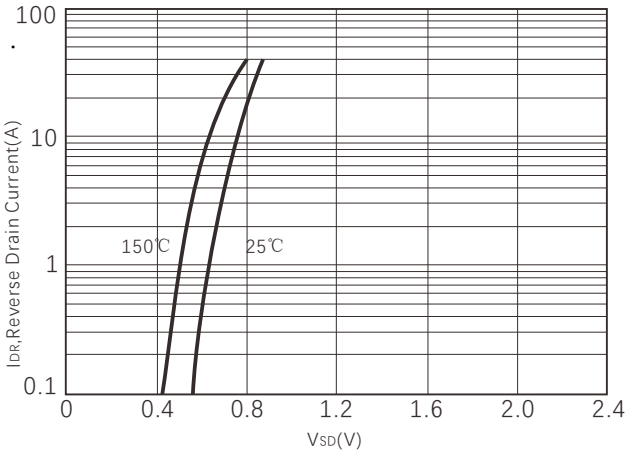


Figure7.Normalized $R_{DS(ON)}$ vs Junction Temperature

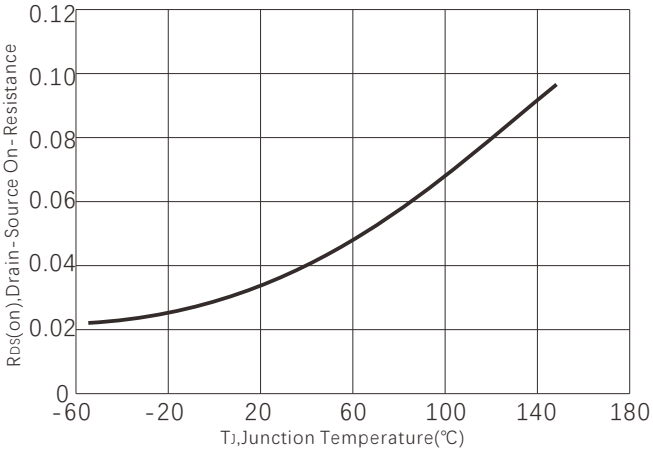


Figure 8.BV_{DSS} vs Junction Temperature

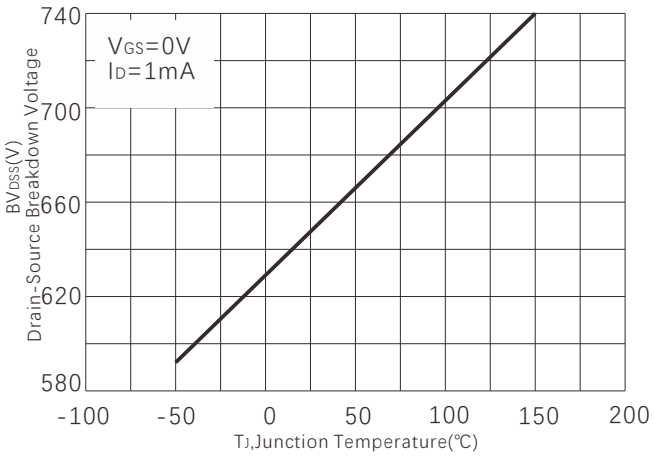


Figure 9. Safe operating area

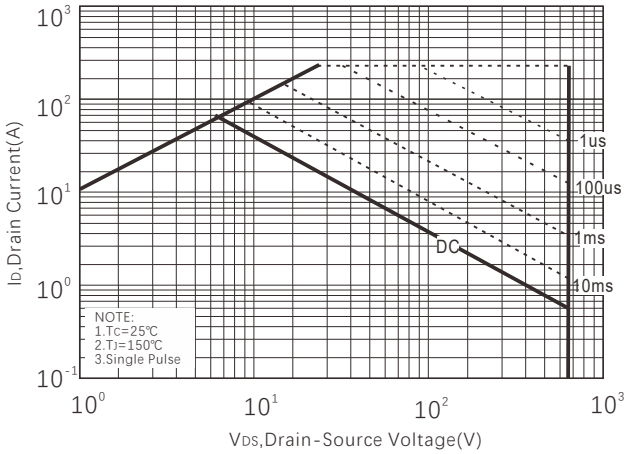


Figure 10. Power dissipation

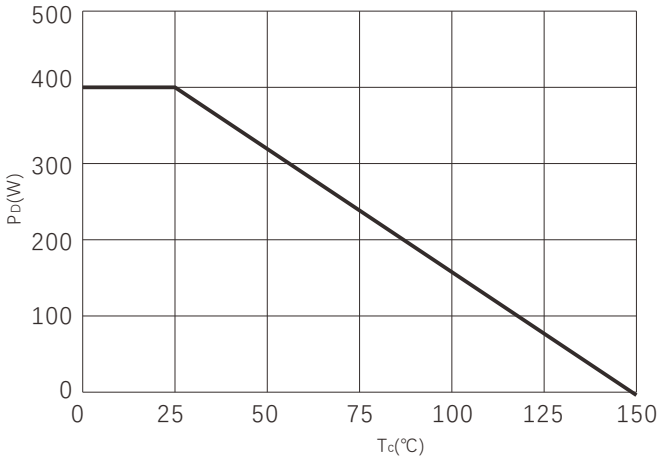
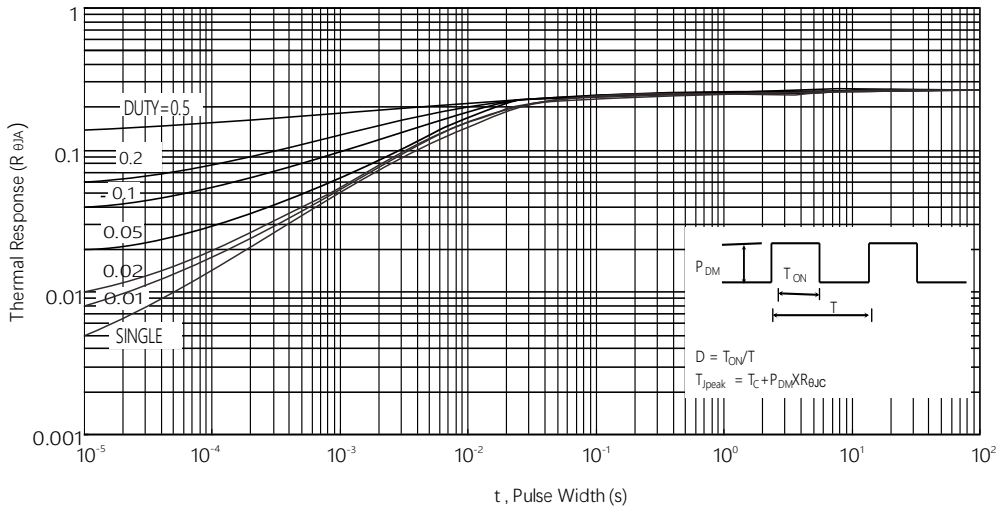
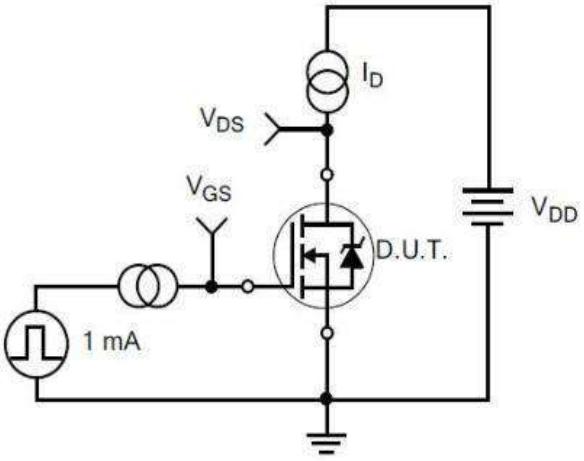


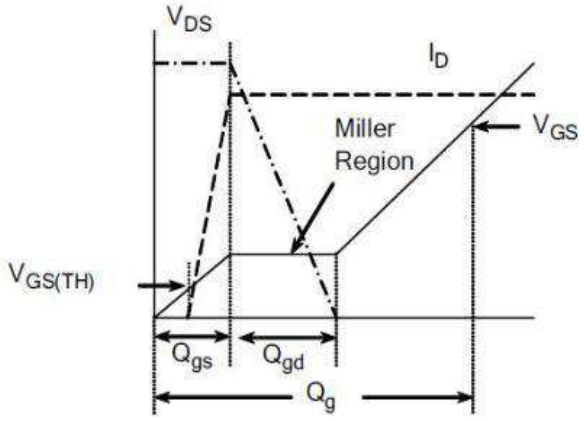
Figure 11. Maximum Transient Thermal Impedance



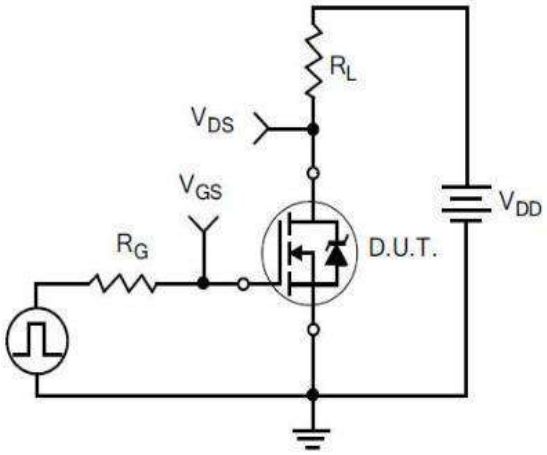
Typical Test Circuit



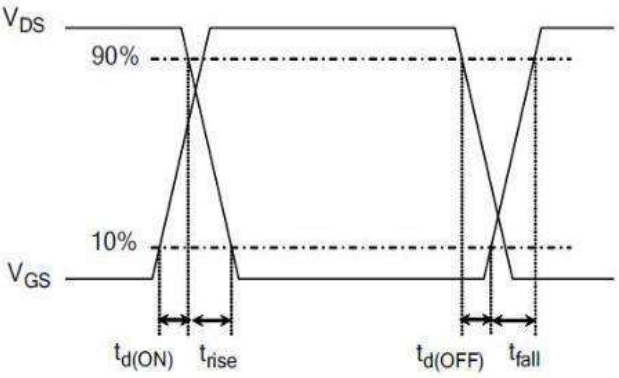
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

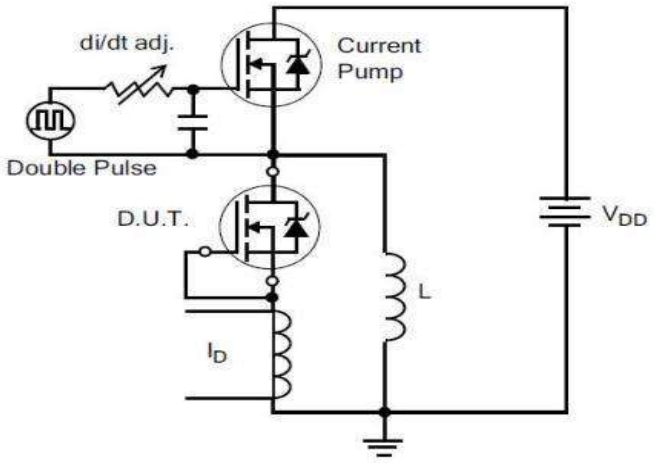


3) Resistive Switching Test Circuit

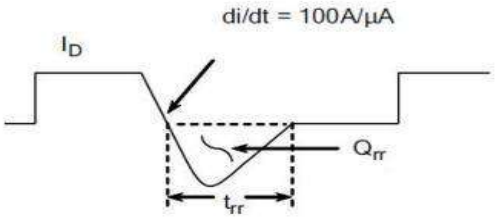


4) Resistive Switching Waveforms

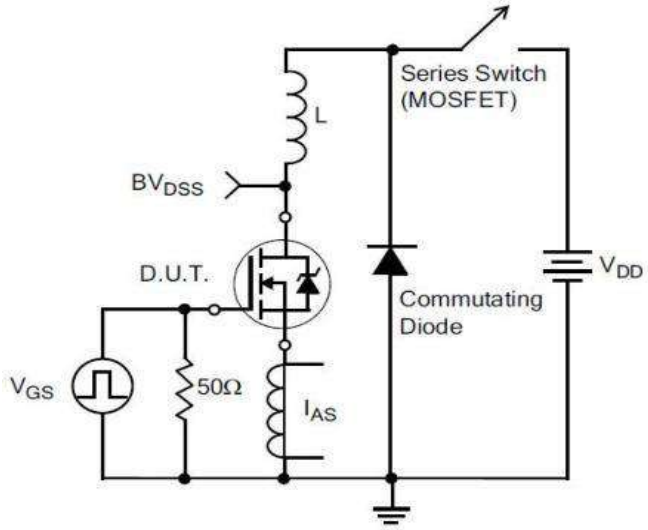
Typical Test Circuit



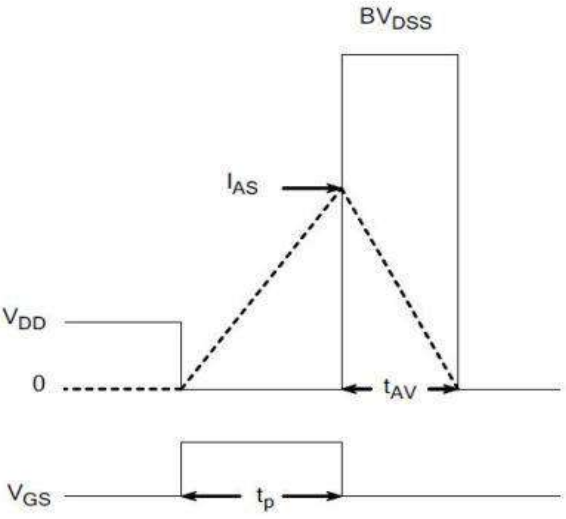
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



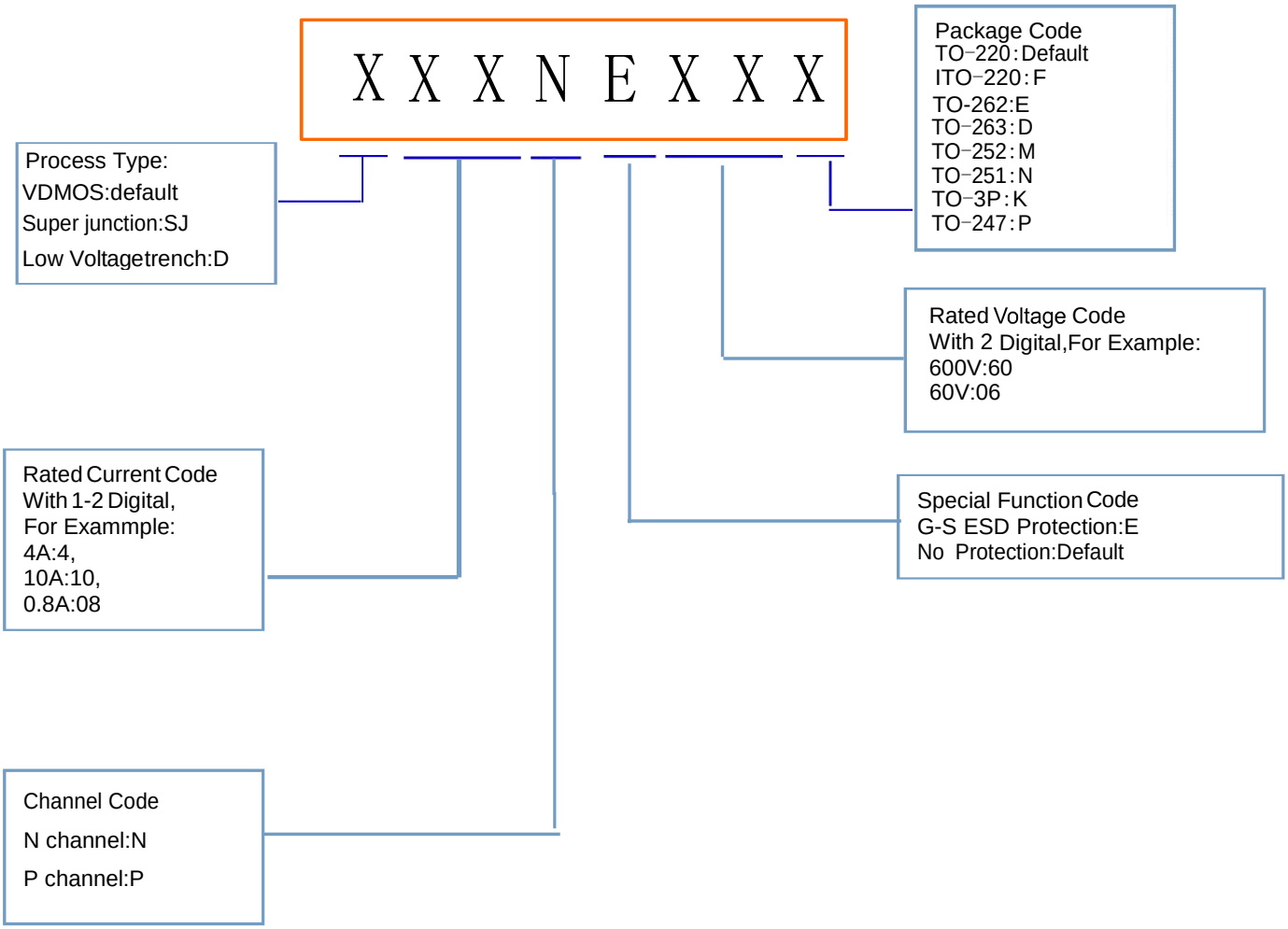
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

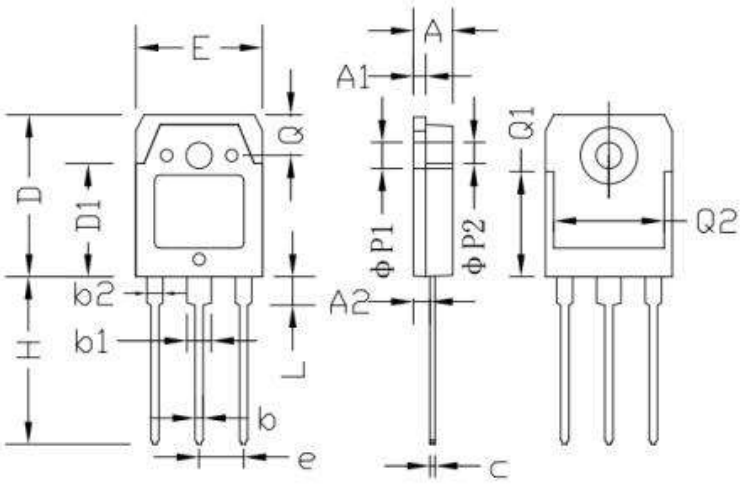
8) Unclamped Inductive Switching Waveforms

Product Names Rules



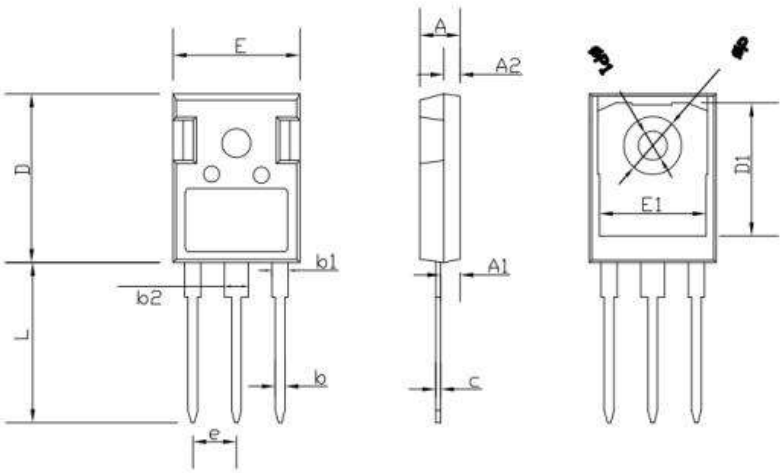
Dimensions

TO-3P PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	4.60	5.00	0.181	0.197
A1	1.45	1.65	0.057	0.065
A2	2.20	2.60	0.087	0.102
b	0.80	1.20	0.032	0.047
b1	2.80	3.20	0.110	0.126
b2	1.80	2.20	0.071	0.087
C	0.55	0.75	0.022	0.030
D	19.20	19.70	0.756	0.776
D1	13.10	14.70	0.516	0.578
E	15.40	15.80	0.607	0.623
e	5.45 TYP		0.215 TYP	
H	19.80	20.20	0.780	0.826
L	3.30	3.70	0.130	0.146
ΦP1	3.20 TYP		0.126 TYP	
ΦP2	3.50 TYP		0.138 TYP	
Q	5.00 TYP		0.197 TYP	
Q1	12.40 TYP		0.488 TYP	
Q2	12.6	-	0.496	-

TO-247 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	4.90	5.10	0.193	0.201
A1	2.31	2.51	0.091	0.099
A2	1.90	2.10	0.075	0.083
b	1.16	1.26	0.046	0.050
b1	1.96	2.06	0.0772	0.0812
b2	2.96	3.06	0.117	0.121
c	0.59	0.66	0.0232	0.0260
D	20.90	21.10	0.8235	0.8313
D1	16.25	16.85	0.6403	0.6639
E	15.70	15.90	0.6186	0.6265
E1	13.10	13.50	0.5161	0.5319
e	5.44		0.2143	
L	19.80	20.10	0.7801	0.7919
ΦP	3.50	3.70	0.1379	0.1458
ΦP1	0	7.30	0	0.2876