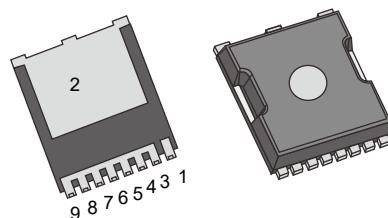


N-Ch 100 V Fast Switching MOSFETs

Features :

- Advanced Trench MOS Technology
- 100% EAS Guaranteed
- Fast Switching Speed
- Green Device Available

TOLL Pin Configuration



Applications :

- Power Tools.
- Motor Control.
- UPS
- Synchronous Rectification in SMPS

Product Summary

BVDSS	RDS(on)	ID
100V	2.2mΩ	308A

Pin Definition:

1. Gate
 2. Drain
- 3/4/5/6/7/8/9. Source

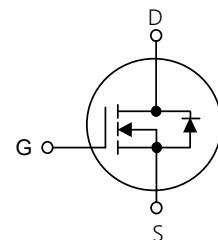


Table1 Absolute Maximum Ratings ($T_C=25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current ^{1,6}	308	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current ^{1,6}	218	A
I_{DM}	Pulsed Drain Current ²	550	A
EAS	Single Pulse Avalanche Energy ³	1012.5	mJ
I_{AS}	Avalanche Current	45	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	429	W
T_{STG}	Storage Temperature Range	-55 to 175	°C
T_J	Operating Junction Temperature Range	-55 to 175	°C

Table 2.Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	60	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	0.35	°C/W

Table 3. Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_D=250\mu\text{A}$	100	---	---	V
$\text{R}_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$\text{V}_{\text{GS}}=10\text{V}$, $\text{I}_D=30\text{A}$	---	1.8	2.2	$\text{m}\Omega$
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{GS}}=\text{V}_{\text{DS}}$, $\text{I}_D=250\mu\text{A}$	2	---	4	V
I_{DSS}	Drain-Source Leakage Current	$\text{V}_{\text{DS}}=80\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$\text{V}_{\text{DS}}=80\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $T_J=100^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$\text{V}_{\text{GS}}=\pm 20\text{V}$, $\text{V}_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$\text{V}_{\text{DS}}=5\text{V}$, $\text{I}_D=20\text{A}$	---	75	---	S
Q_g	Total Gate Charge	$\text{V}_{\text{DS}}=50\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{I}_D=20\text{A}$	---	200	---	nC
Q_{gs}	Gate-Source Charge		---	53.3	---	
Q_{gd}	Gate-Drain Charge		---	49	---	
$\text{T}_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}}=50\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{R}_G=3\Omega$, $\text{I}_D=20\text{A}$	---	47	---	ns
T_r	Rise Time		---	28	---	
$\text{T}_{\text{d(off)}}$	Turn-Off Delay Time		---	79	---	
T_f	Fall Time		---	18	---	
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=50\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	13362	---	pF
C_{oss}	Output Capacitance		---	1917	---	
C_{rss}	Reverse Transfer Capacitance		---	387	---	

Diode Characteristics

I_s	Continuous Source Current ^{1,5,6}	$\text{V}_G=\text{V}_D=0\text{V}$, Force Current	---	---	80	A
V_{SD}	Diode Forward Voltage ²	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.1	V
t_{rr}	Reverse Recovery Time	$\text{I}_F=20\text{A}$, $d\text{i}/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	70	---	nS
Q_{rr}	Reverse Recovery Charge		---	580	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $\text{V}_{\text{DD}}=50\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $L=1.0\text{mH}$, $\text{I}_{\text{AS}}=45\text{A}$
- 4.The power dissipation is limited by 175°C junction temperature
- 5.The data is theoretically the same as I_D and I_s , in real applications , should be limited by total power dissipation.
6. Bonding wire limitation current is 120A.

Typical Characteristics

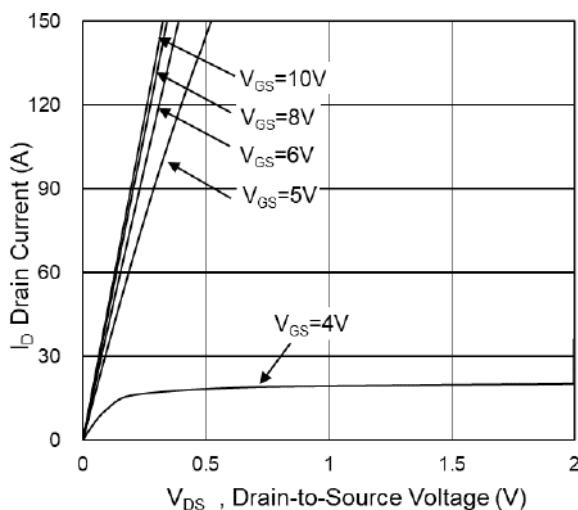


Fig.1 Typical Output Characteristics

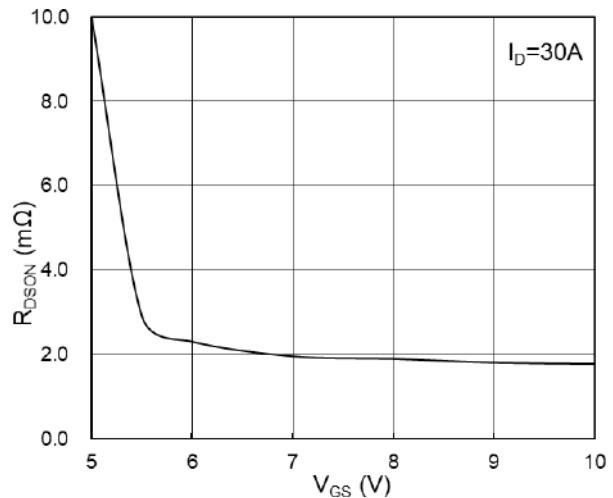


Fig.2 On-Resistance vs G-S Voltage

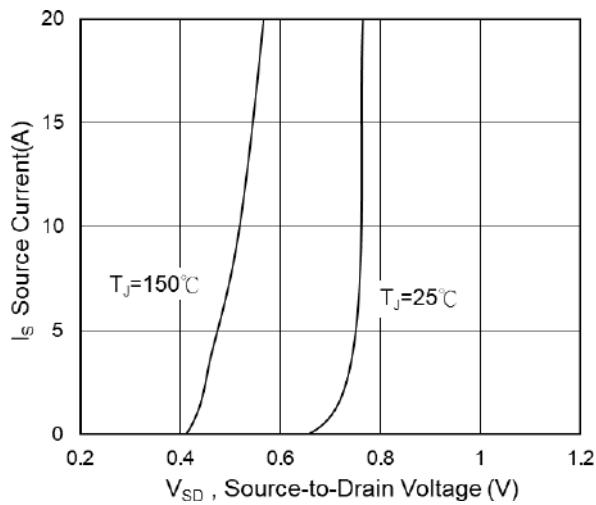


Fig.3 Source-Drain Forward Characteristics

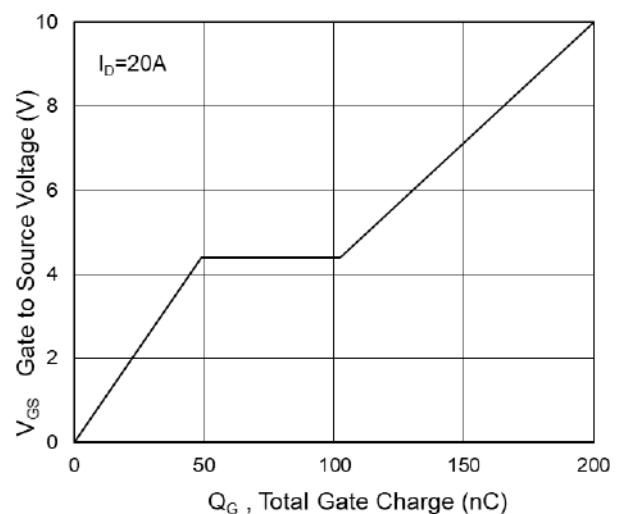


Fig.4 Gate-Charge Characteristics

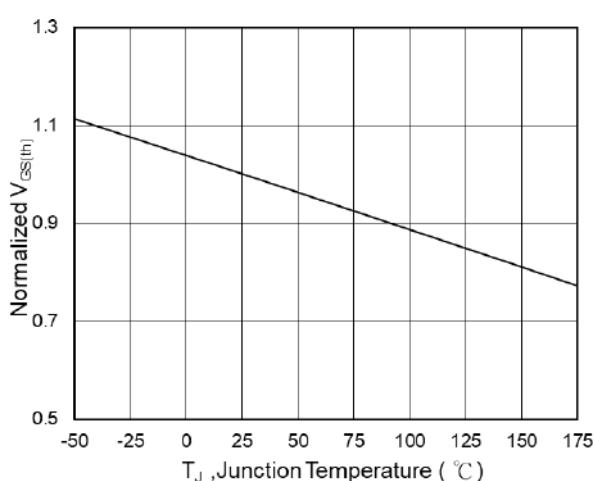


Fig.5 Normalized V_{GS(th)} vs T_J

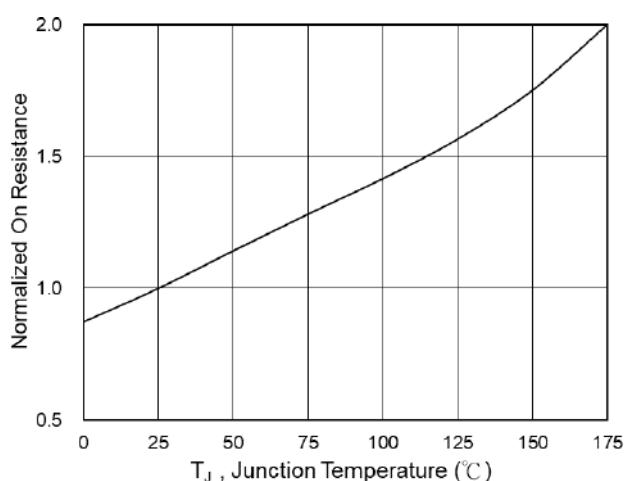


Fig.6 Normalized R_{DS(on)} vs T_J

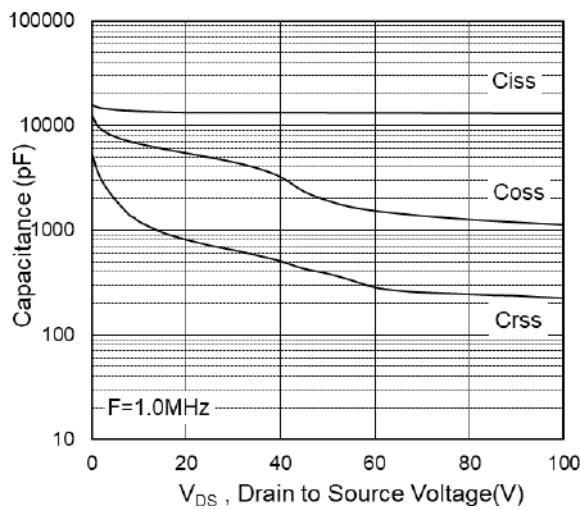


Fig.7 Capacitance

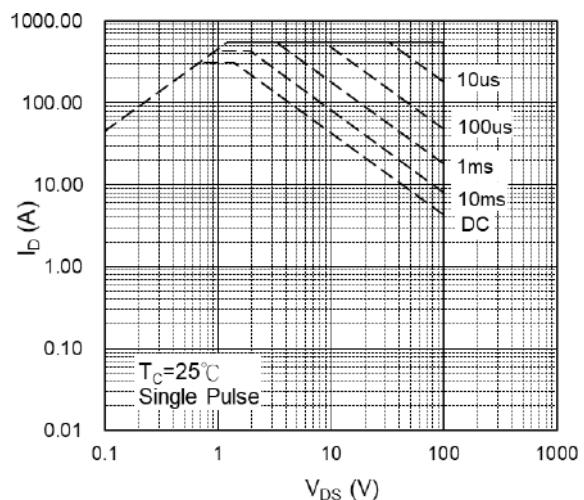


Fig.8 Safe Operating Area

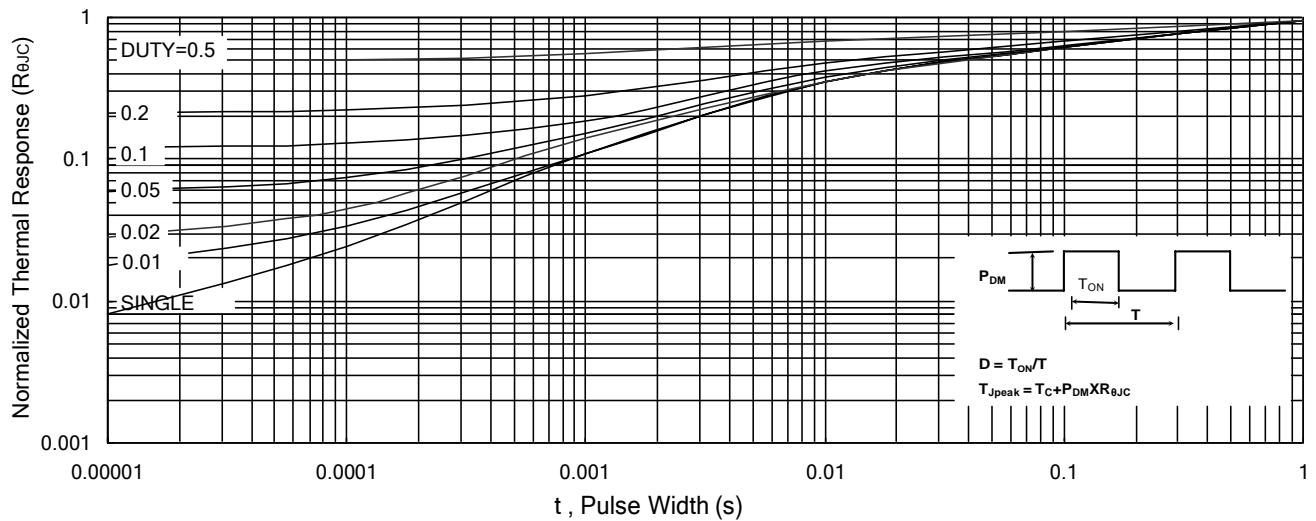


Fig.9 Normalized Maximum Transient Thermal Impedance

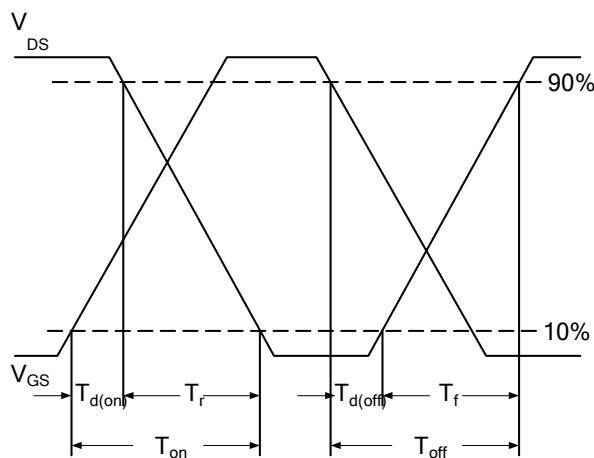


Fig.10 Switching Time Waveform

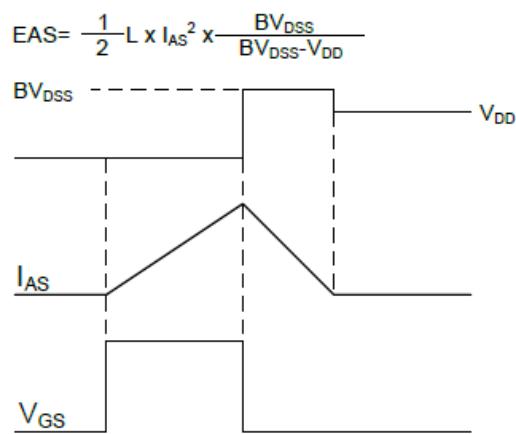
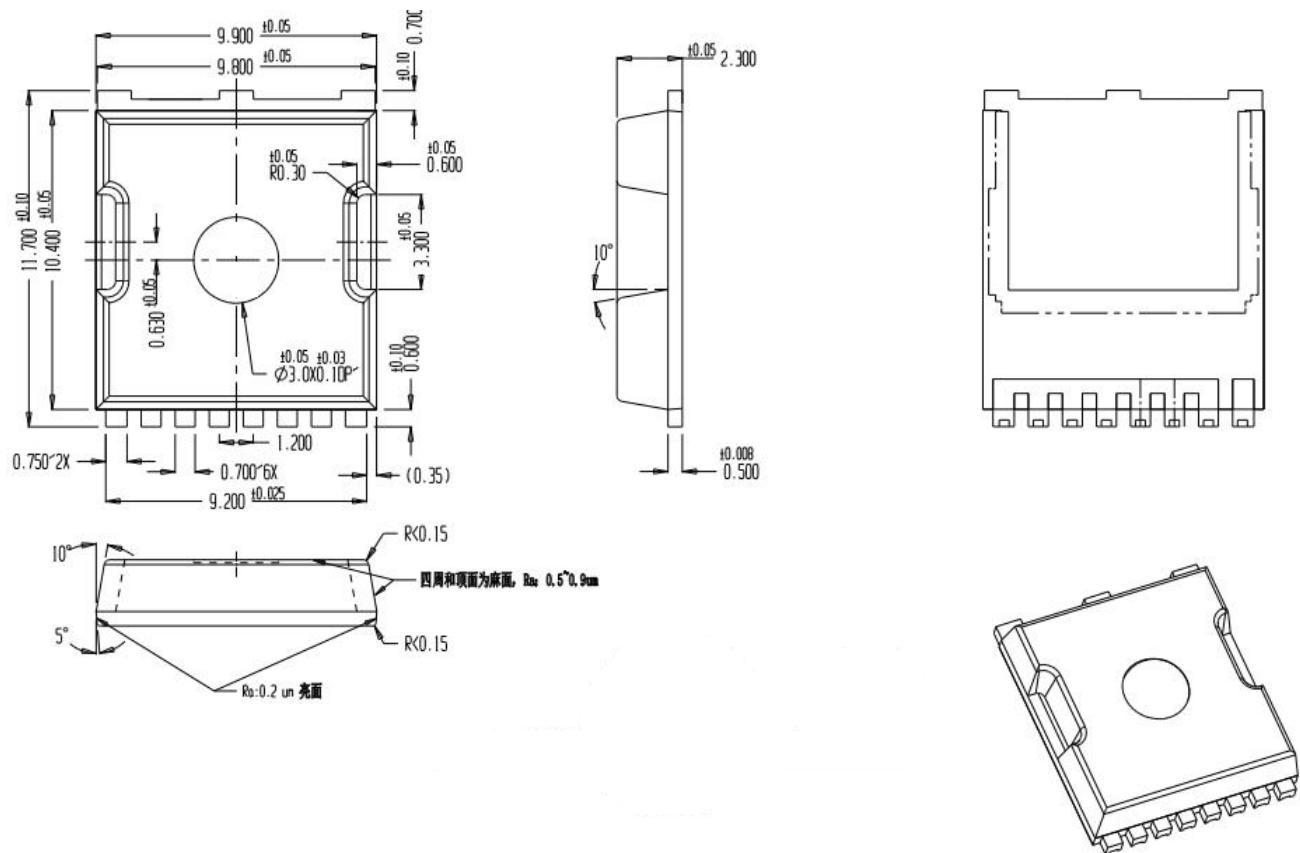


Fig.11 Unclamped Inductive Switching Waveform

Dimensions

TOLL PACKAGE OUTLINE DIMENSIONS



Suggested Pad Layout

