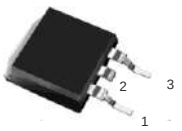
1000V Silicon N-Channel Power MOSFET

Description:

KJ4N100M the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252, which accords with the RoHS standard.

TO-252



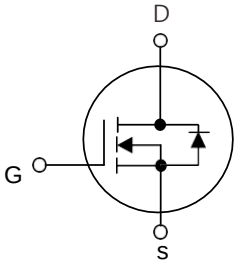
Features:

- Low on-resistance
- Low gate charge and Fast Switching
- 100% avalanche tested
- Rohs compliant

Block Diagram

Pin Definition:

1.Gate
2.Drain
3.Source



Mechanical Data:

- Case:TO-252 Package

Application:

- Power switch circuit of adaptor and charger

Product Summary			
V_{DS}	$R_{DS(on)}$(Ω)Typ	I_D(A)	Qg(Typ)
1000V	4.5 @ 10V,2A	4	17nc

Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameters		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	1000	V
Gate-Source Voltage		V_{GS}	±30	V
Contionous Drain Current	T_C=25°C	I_D	4	A
	T_C=100°C		2.4	
Pulsed Drain Current (Note 1)		I_{DM}	16	A
Single Pulse Avalanche Energy(Note 2)		EAS	180	mJ
Reverse Diode Recovery dv/dt(Note 3)		dv/dt	5.0	V/ns
Power Dissipation T_C=25°C		P_D	75	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55 ~ +150	℃

Table 2.Thermal Characteristics

Parameters	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	83.3	℃/W
Thermal resistance Junction to Case	$R_{\theta JC}$	1.67	℃/W

Table 3. Electrical Chatacteristics (T_J=25℃, unless otherwise specified)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	1000			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=1000V,V_{GS}=0V			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V			100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V			-100	nA
On Characteristics(Note 4)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=2A		4.5	5.5	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1MHz		850		pF
Output Capacitance		C_{OSS}			66		pF
Reverse Transfer Capacitance		C_{RSS}			23		pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V_{DD}=500V,I_D=4A, V_{GS}=10V,R_G=12Ω		17		ns
Turn-On Rise Time		tr			6		ns
Turn-Off Delay Time		td(off)			23		ns
Turn-Off Fall Time		tf			11		ns
Total Gate Charge		Q_G	V_{DS}=500V,I_D=4A, V_{GS}=10V		17		nC
Gate-Source Charge		Q_{GS}			4.5		nC
Gate-Drain Charge		Q_{GD}			5.6		nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V,I_S=4A			1.5	V
Maximum Continuous Drain-Source Diode Forward Current(Note 4)		I_S				4	A
Reverse Recovery Time		trr	V_{GS}=0V,I_S=4A dI$_F$/dt=100A/μs(Note 4)		220		ns
Reverse Recovery Charge		Q_{RR}			0.95		μC

Notes：1 Repetitive Rating:Pulse width limited by maximum junction temperature 2
L=10mH,I_D=6.0A,Starting T_J=25°C
3 I_{SD}=4A,di/dt≤100A/μS,V_{DD}≤BV_{DSS},starting T_J=25℃
4 Pulse Test: Pulse width ≤300μS,Duty cycle≤2%5
Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

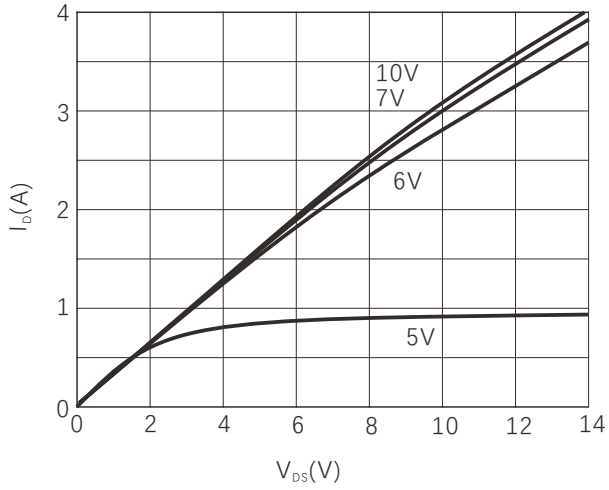


Figure 2.$R_{DS(ON)}$ vs Junction Temperature

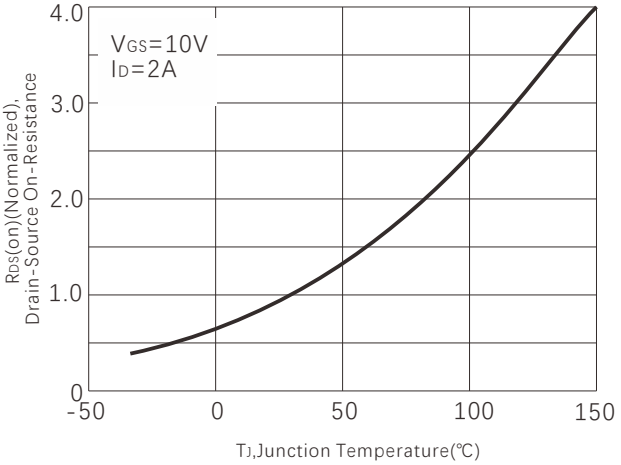


Figure 3.$R_{DS(on)}$ Normalized to I_D=2A vs.Drain Current

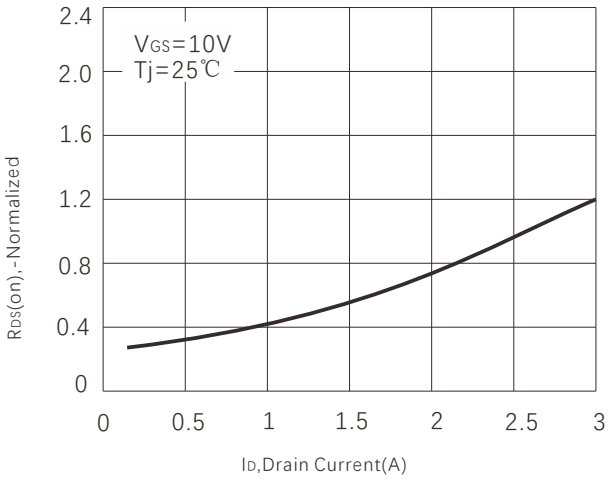


Figure 4. Capacitance

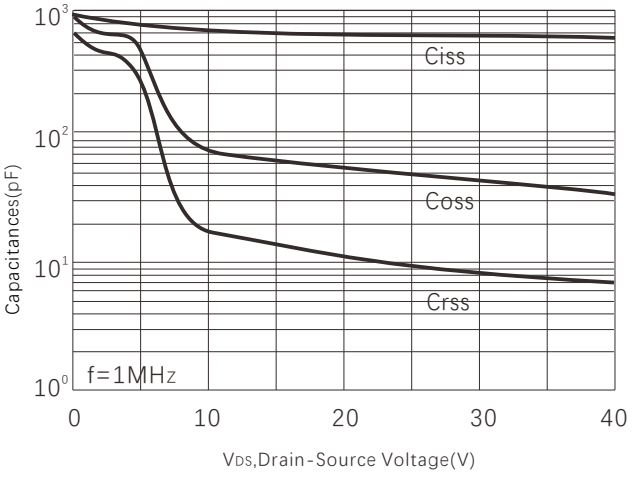


Figure 5.Gate charge

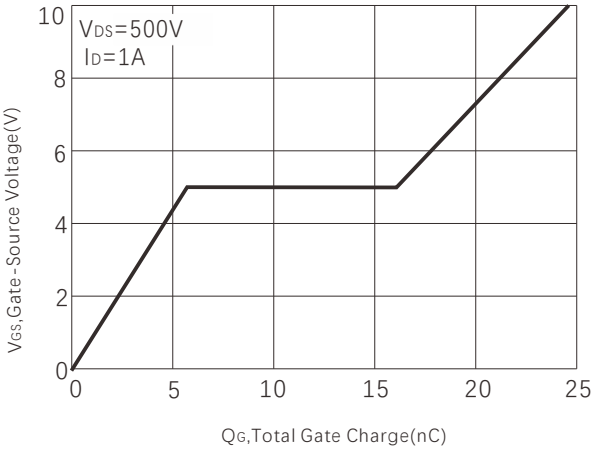


Figure 6. Typical Body Diode Transfer Characteristics

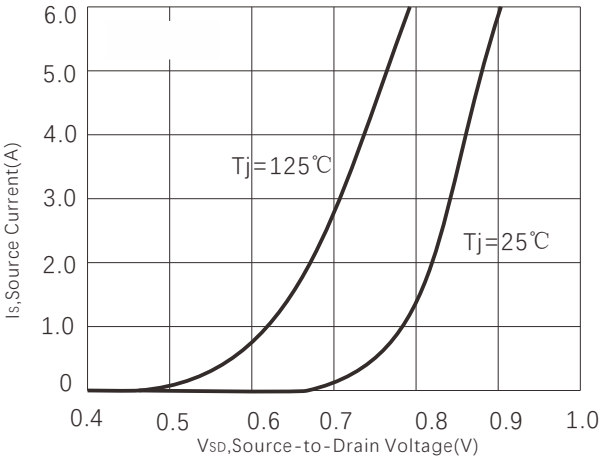


Figure7.$R_{DS(ON)}$ vs Junction Temperature

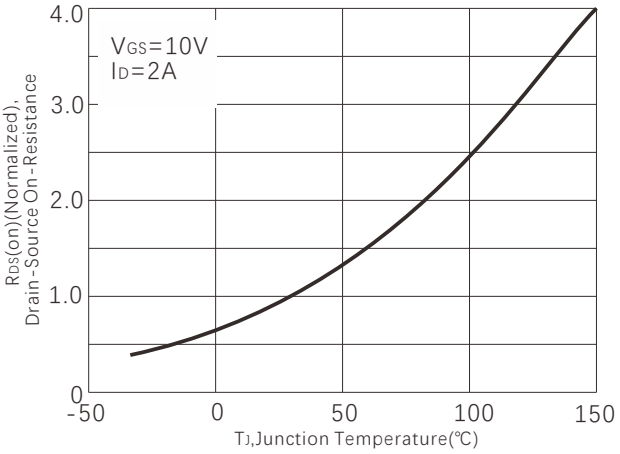


Figure 8. Safe operating area

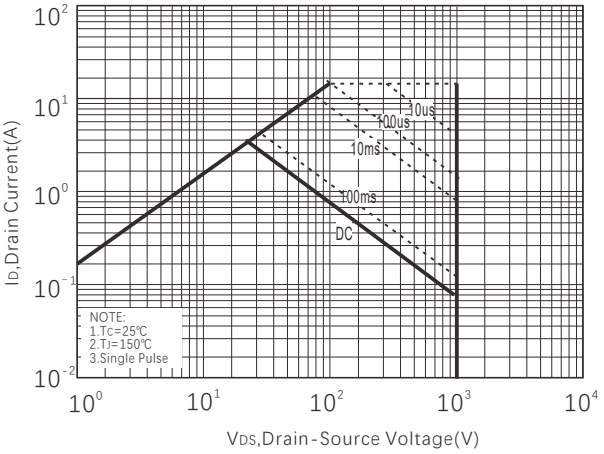
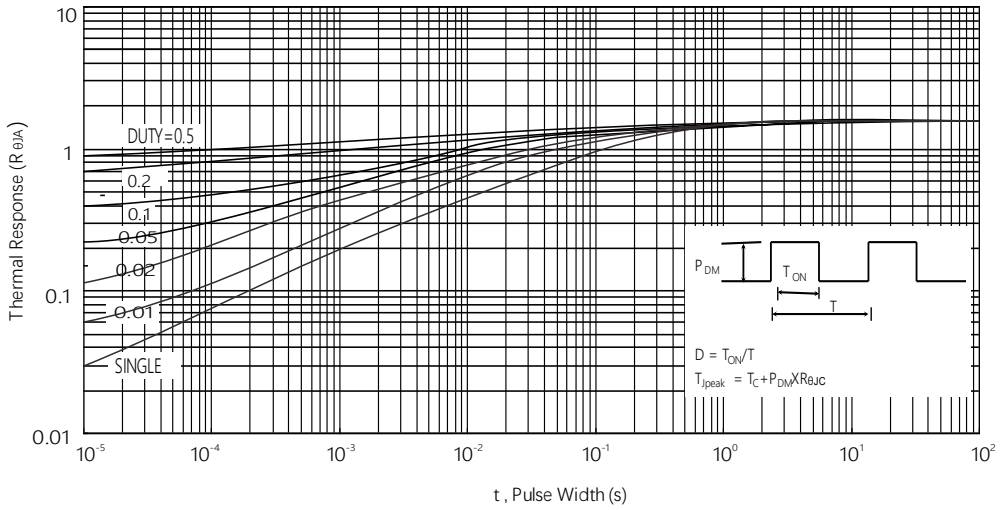
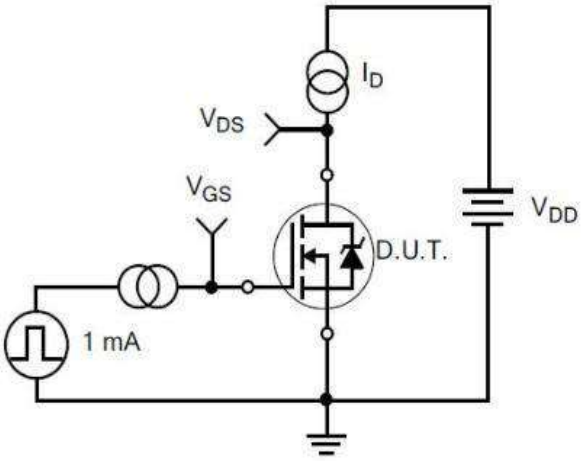


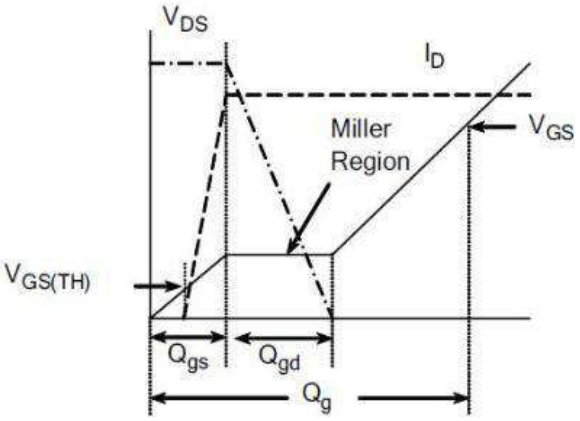
Figure 9. Maximum Transient Thermal Impedance



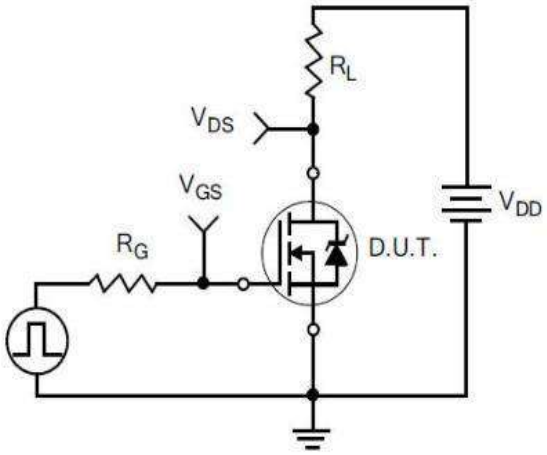
Typical Test Circuit



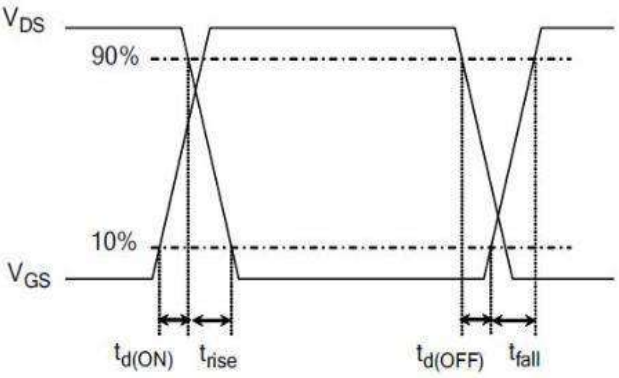
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

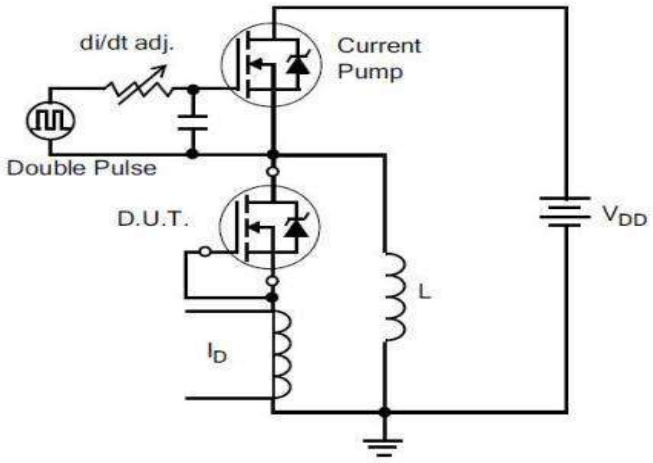


3) Resistive Switching Test Circuit

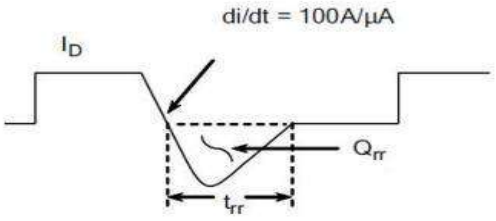


4) Resistive Switching Waveforms

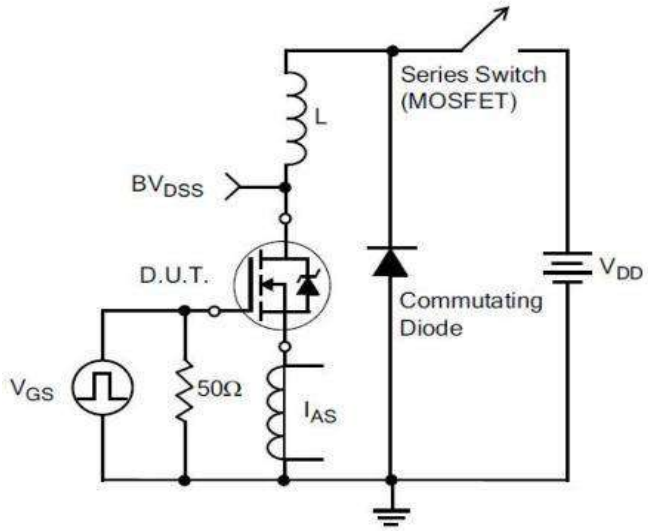
Typical Test Circuit



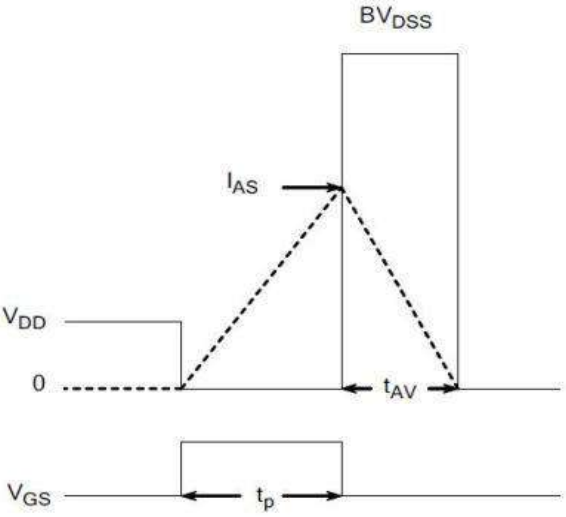
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



7) . Unclamped Inductive Switching Test Circuit

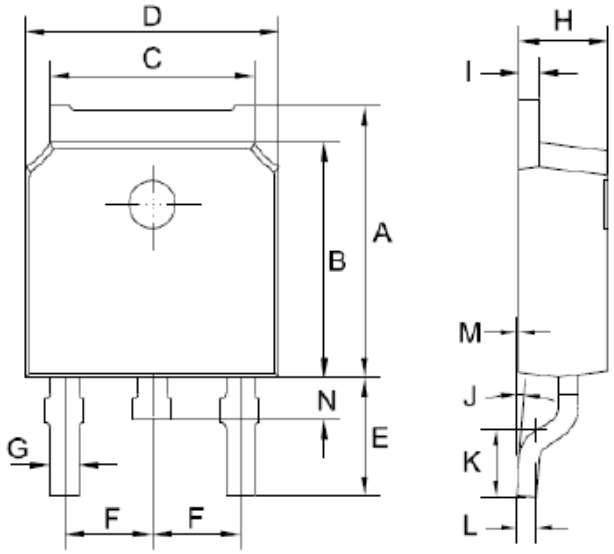


$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

8) Unclamped Inductive Switching Waveforms

Dimensions

TO-252 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	6.85	7.25	0.270	0.285
B	5.8	6.3	0.228	0.248
C	5	5.53	0.197	0.218
D	6.3	6.8	0.248	0.268
E	2.6	3.3	0.102	0.130
F	2.19	2.39	0.086	0.094
G	0.45	0.85	0.018	0.033
H	2.2	2.4	0.087	0.094
I	0.41	0.61	0.016	0.024
J	0°	8°	0°	8°
K	1.45	1.85	0.057	0.073
L	0.41	0.61	0.016	0.024
M	0	0.12	0.000	0.005
P	0.6	1	0.024	0.039