

N - Channel 60V (D-S) MOSFET, ESD Protection

Features:

- $R_{DS(ON)} \leq 4\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 4\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

Applications:

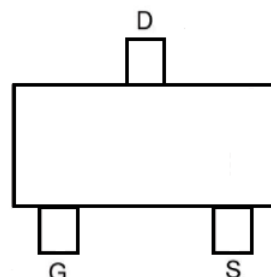
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch

GENERAL DESCRIPTION

The KW2N7002E-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

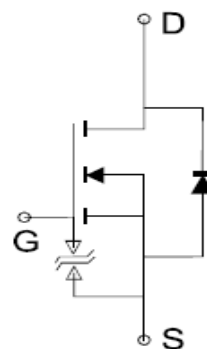
(SOT-23)

Top View



Ordering Information:

KW2N7002E-G (Green product-Halogen free)



N-Channel MOSFET

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain	$T_A=25^\circ\text{C}$	I_D	0.24	A
	$T_A=70^\circ\text{C}$	I_D	0.19	
Pulsed Drain Current		I_{DM}	0.9	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	0.36	W
	$T_A=70^\circ\text{C}$	P_D	0.23	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	350	$^\circ\text{C/W}$

* The device mounted on 1in² FR4 board with 2 oz copper

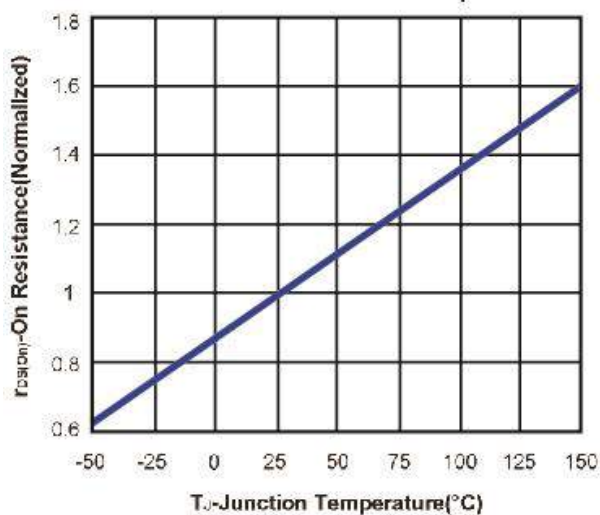
Electrical Characteristics ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	1		2	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} = $\pm$ 20V			$\pm$ 1	μ A
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =500mA		1.8	4	Ω
		V _{GS} =4.5V, I _D =200mA		2.1	4	
V _{SD}	Diode Forward Voltage *	I _{SD} =200mA, V _{GS} =0V		1	1.3	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =25V, V _{GS} =10V, I _D =0.22A		4.7	6	nC
Q _{gs}	Gate-Source Charge			2.3	3.5	
Q _{gd}	Gate-Drain Charge			0.9	1.5	
R _g	Gate Resistance	f=1MHz			700	Ω
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		23.2	40	pF
C _{oss}	Output Capacitance			2.6	5	
C _{rss}	Reverse Transfer Capacitance			1.6	3	
t _{d(on)}	Turn-On Delay Time	V _{DD} =30V, R _L =103 Ω I _D =0.29A, V _{GS} =10V, R _{GEN} =6 Ω		5.4	10	ns
t _r	Turn-On Rise Time			3.6	7	
t _{d(off)}	Turn-Off Delay Time			24.3	40	
t _f	Turn-Off Fall Time			14.5	30	

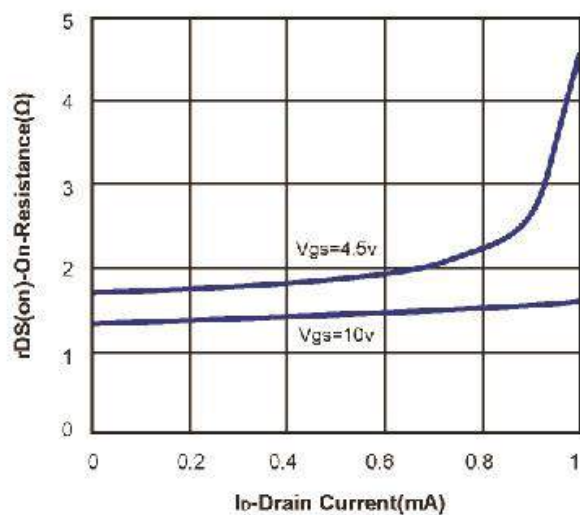
Notes: a, pulse test: pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ reserves the right to improve product design, functions and reliability without notice.

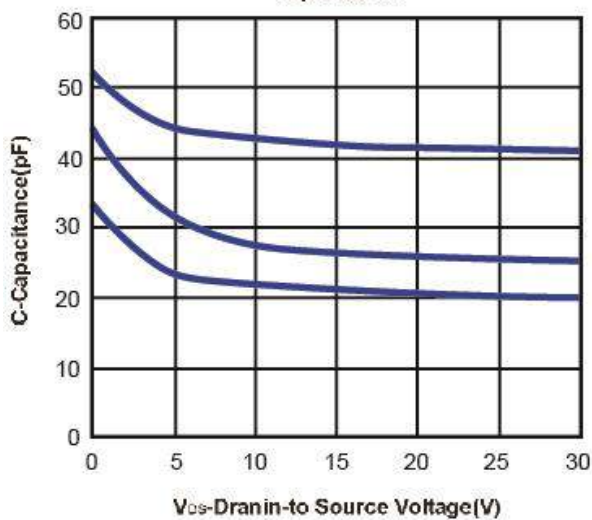
On Resistance vs. Junction Temperature



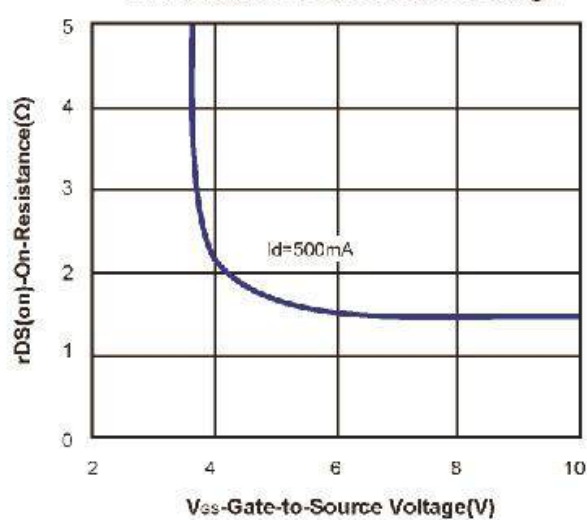
On Resistance vs. Drain Current



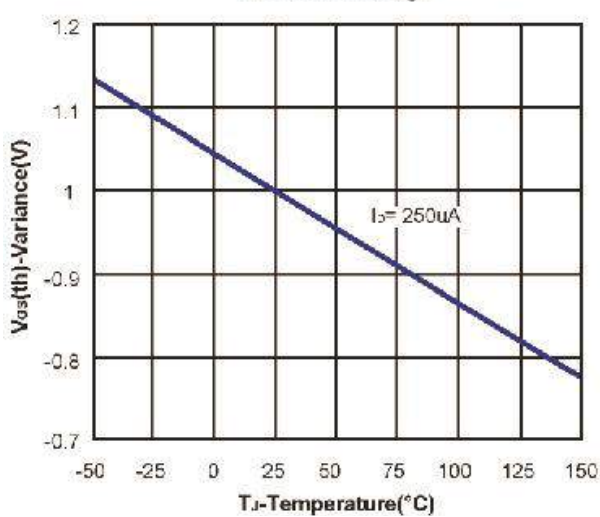
Capacitance



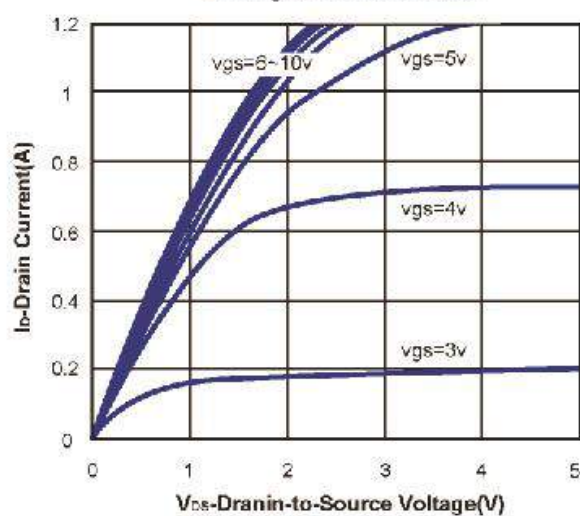
On Resistance vs. Gate-to-Source Voltage

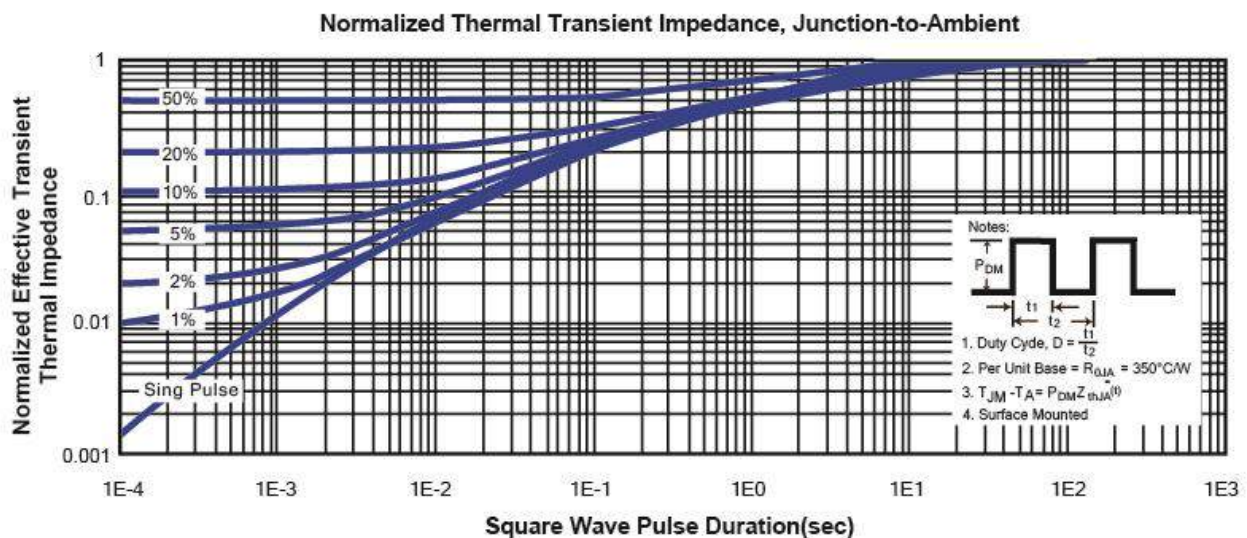
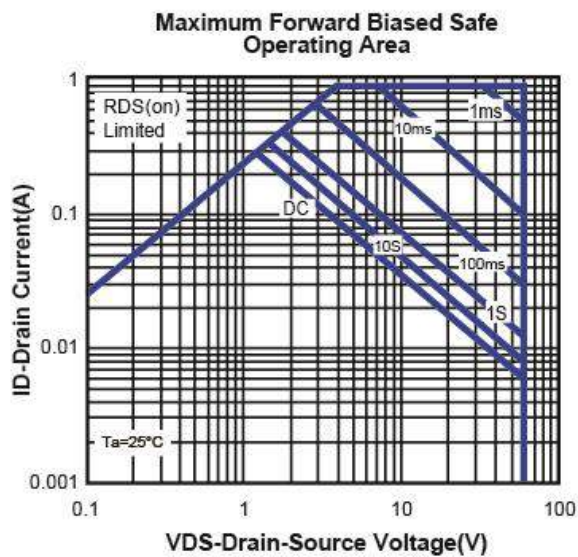
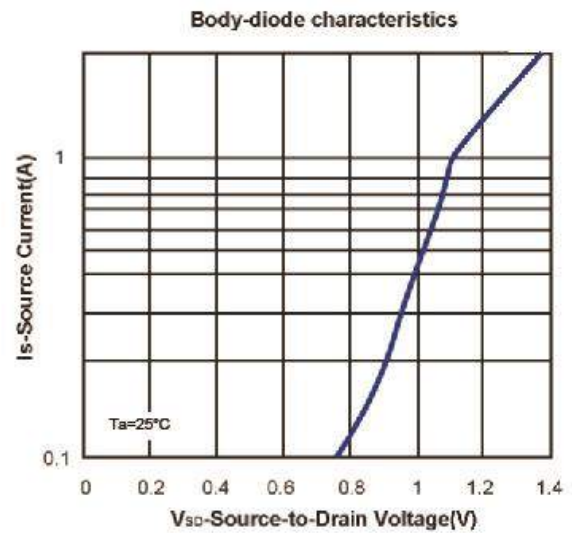
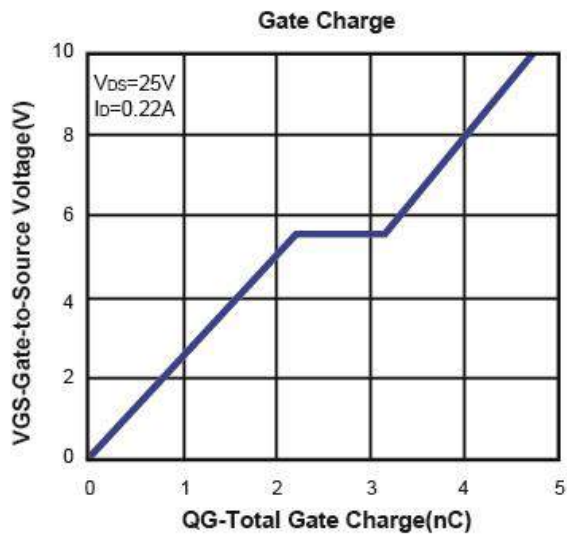


Threshold Voltage

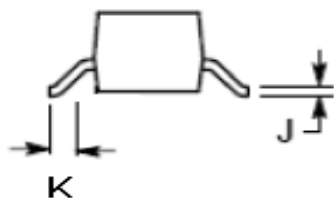
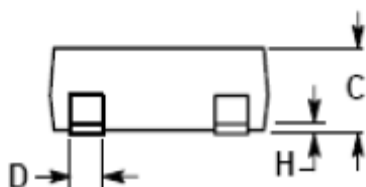
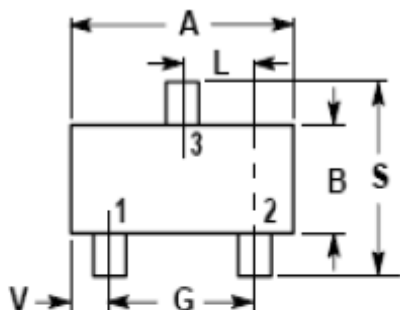


On-Region Characteristics





SOT-23 Package Outline

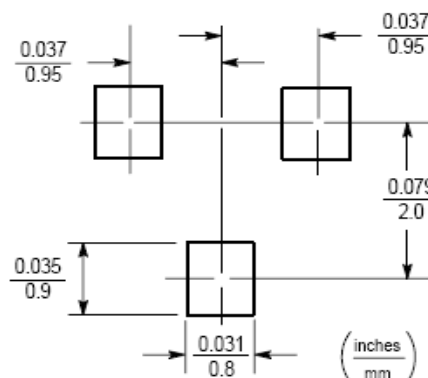


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.5
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.007	—	0.018	—
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

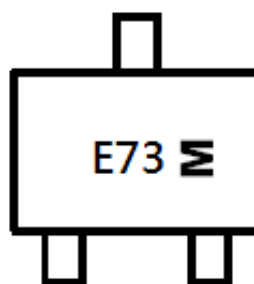
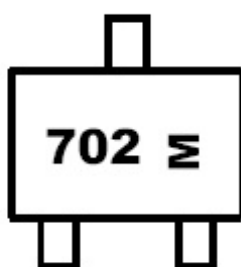
SOLDERING FOOTPRINT*



Device name: KW2N7002E-G

Package: SOT-23

Marking Code :



702&E73: Device Marking
 Code M: Date code

MONTH CODE

ODD YEARS(2007, 2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z