

## 200V N-Ch Power MOSFET

### Feature

- ◇ High Speed Power Smooth Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free

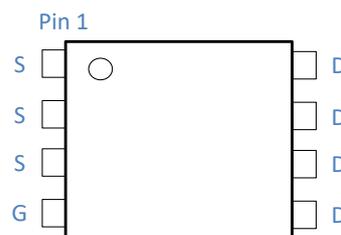
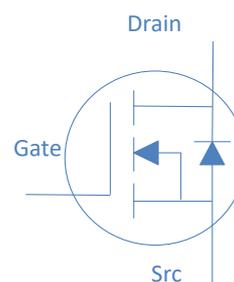
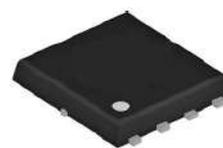
### Application

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control

Part Number	Package	Marking
KSPRGM1K2N20ML	DFN 3.3*3.3	M1K2N20L

$V_{DS}$	200	V
$R_{DS(on),typ}$ $V_{GS}=10V$	104	m $\Omega$
$R_{DS(on),typ}$ $V_{GS}=4.5V$	114	m $\Omega$
$I_D$ (Silicon Limited)	13	A
$I_D$ (Package Limited)	10	A

DFN3.3\*3.3



### Absolute Maximum Ratings at $T_J=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^\circ\text{C}$	13	A
		$T_C=100^\circ\text{C}$	9.2	
		Continuous Drain Current (Package Limited)	$T_C=25^\circ\text{C}$	
Drain to Source Voltage	$V_{DS}$	-	200	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	25	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.4\text{mH}, T_C=25^\circ\text{C}$	5	mJ
Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	40	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	$^\circ\text{C}$

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	3.1	$^\circ\text{C/W}$
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	65	$^\circ\text{C/W}$

**Electrical Characteristics at T<sub>j</sub>=25°C (unless otherwise specified)**

**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	200	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	1	2	3	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =200V, T <sub>j</sub> =25°C	-	-	1	μA
		V <sub>GS</sub> =0V, V <sub>DS</sub> =200V, T <sub>j</sub> =100°C	-	-	100	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Drain to Source on Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5A	-	104	120	mΩ
	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A	-	114	140	mΩ
Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	-	15	-	S
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> Open, f=1MHz	-	5.5	-	Ω

**Dynamic Characteristics**

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz	-	491	-	pF
Output Capacitance	C <sub>oss</sub>		-	22	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	5.5	-	
Total Gate Charge	Q <sub>g</sub> (10V)	V <sub>DD</sub> =100V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V	-	9.8	-	nC
Total Gate Charge	Q <sub>g</sub> (4.5V)		-	5.8	-	
Gate to Source Charge	Q <sub>gs</sub>		-	1.6	-	
Gate to Drain (Miller) Charge	Q <sub>gd</sub>		-	3.2	-	
Turn on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =100V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V, R <sub>G</sub> =10Ω,	-	9	-	ns
Rise time	t <sub>r</sub>		-	5	-	
Turn off Delay Time	t <sub>d(off)</sub>		-	13	-	
Fall Time	t <sub>f</sub>		-	4	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>F</sub> =20A	-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>R</sub> =100V, I <sub>F</sub> =5A, dI <sub>F</sub> /dt=100A/μs	-	60	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>		-	126	-	nC

Fig 1. Typical Output Characteristics

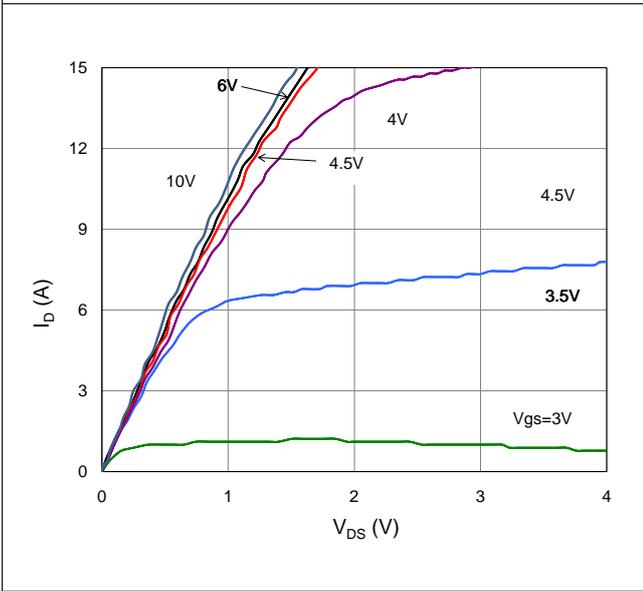


Figure 2. On-Resistance vs. Gate-Source Voltage

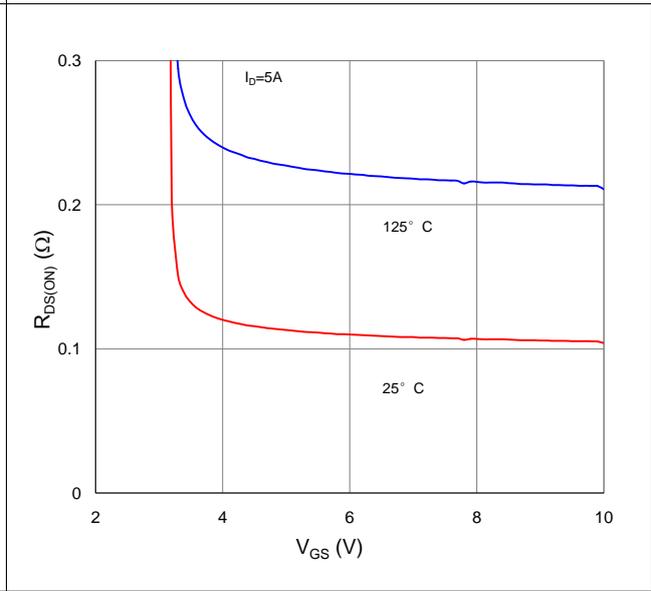


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

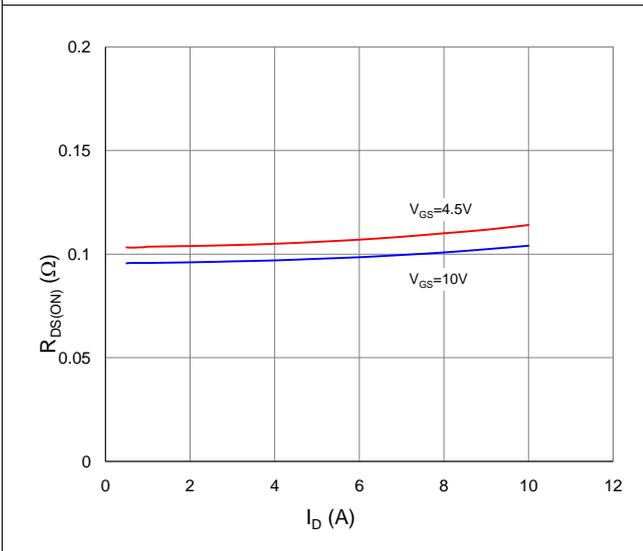


Figure 4. Normalized On-Resistance vs. Junction Temperature

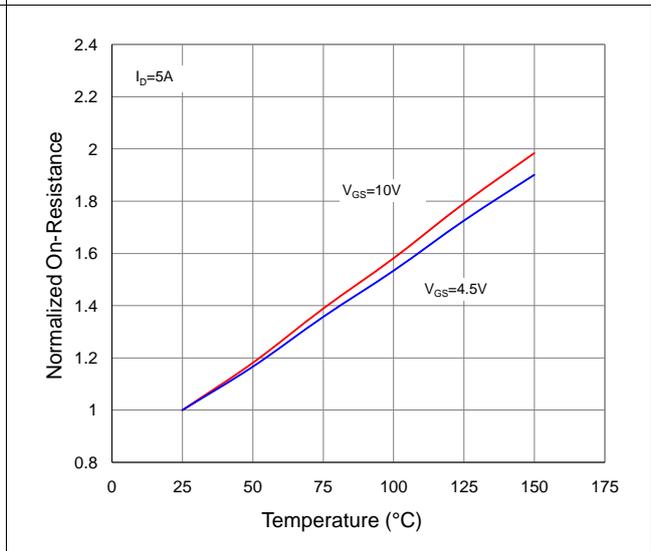


Figure 5. Typical Transfer Characteristics

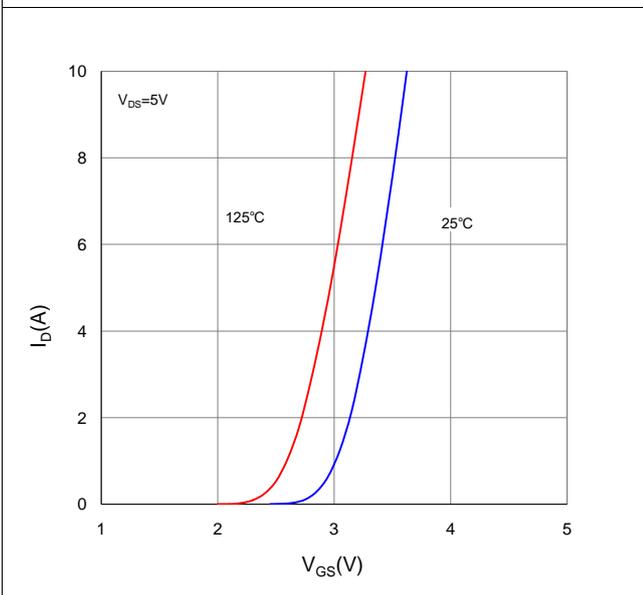


Figure 6. Typical Source-Drain Diode Forward Voltage

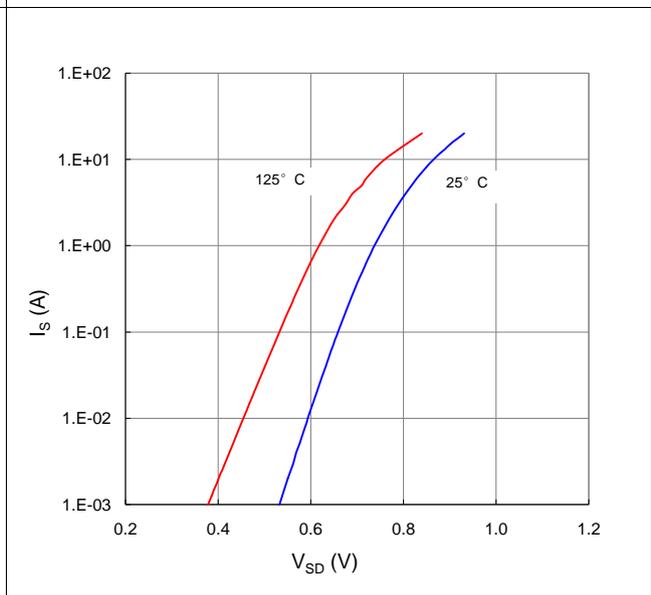


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

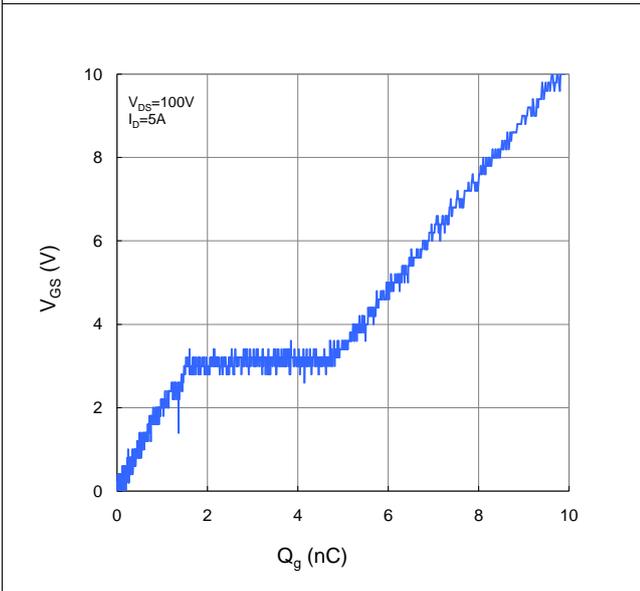


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

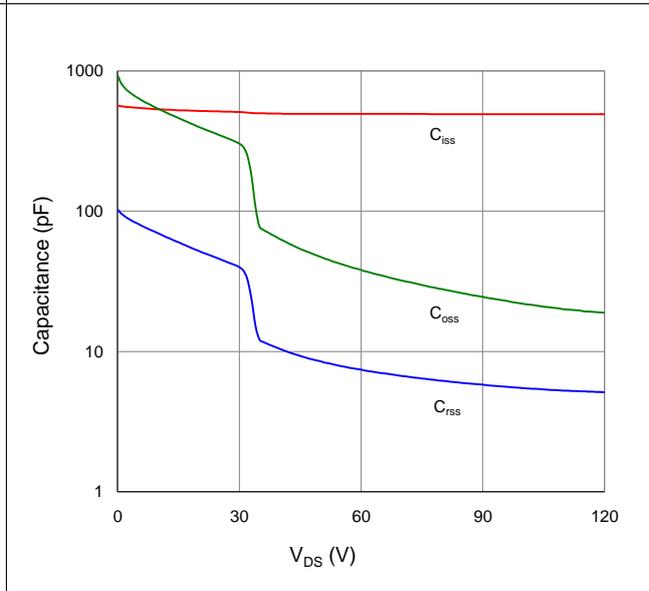


Figure 9. Maximum Safe Operating Area

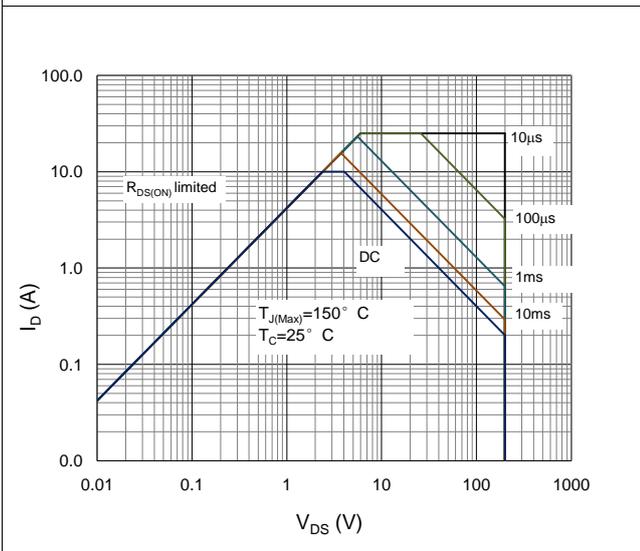


Figure 10. Maximum Drain Current vs. Case Temperature

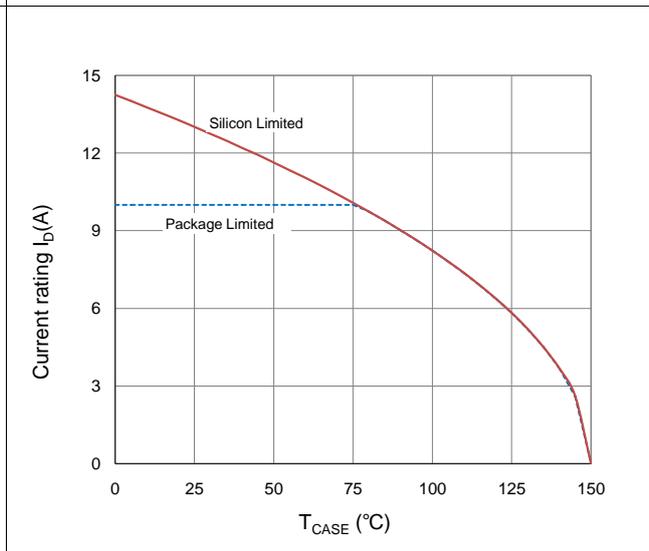
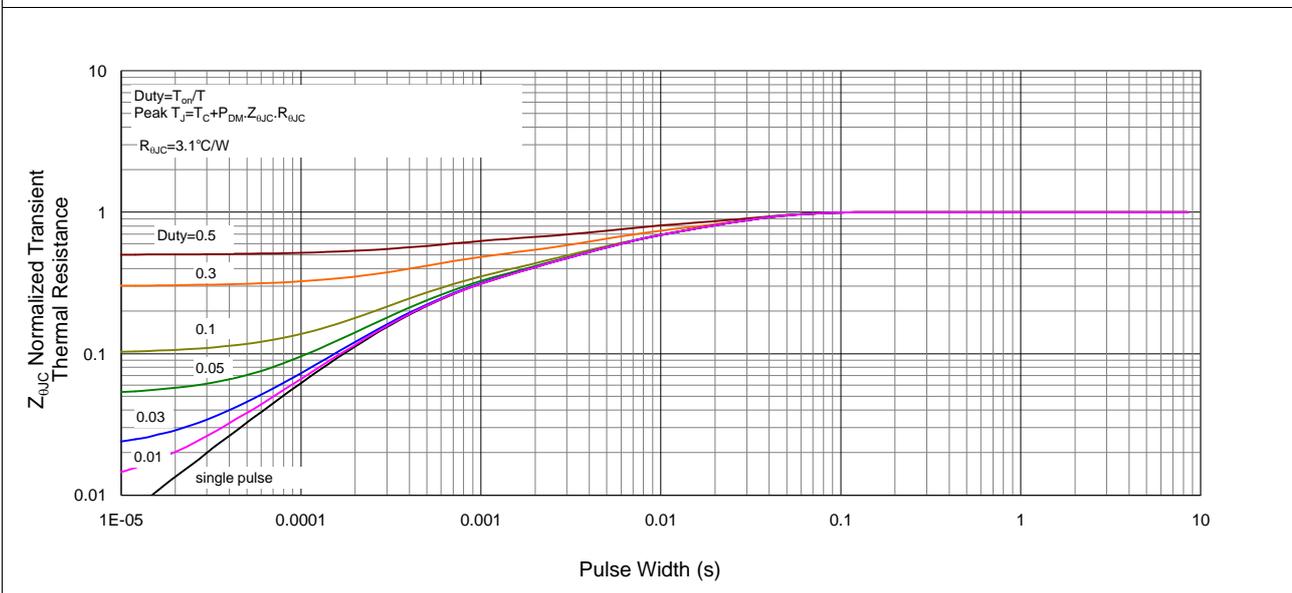
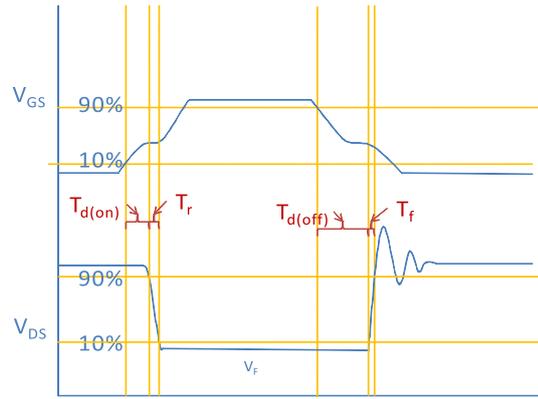
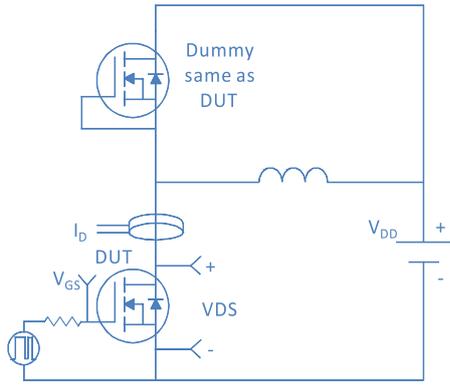


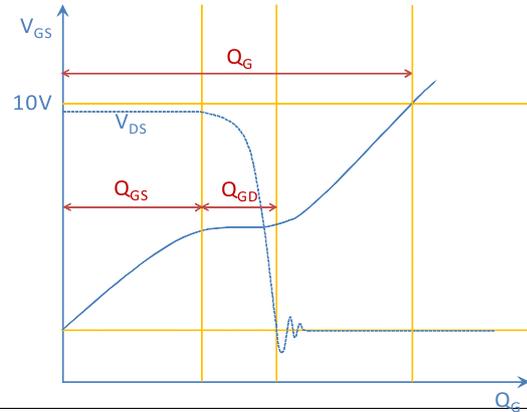
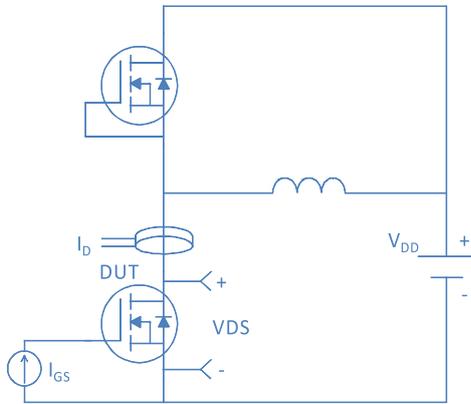
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



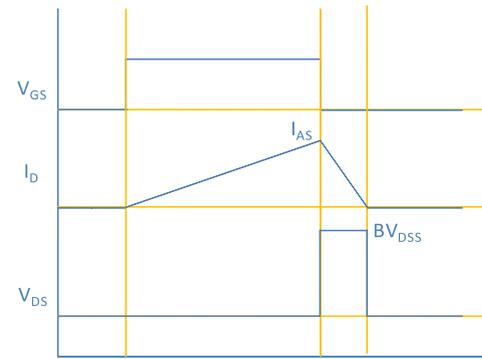
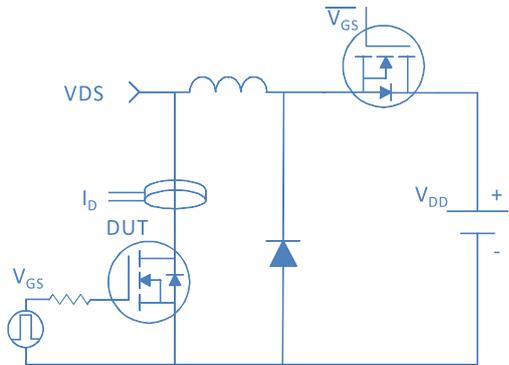
**Inductive switching Test**



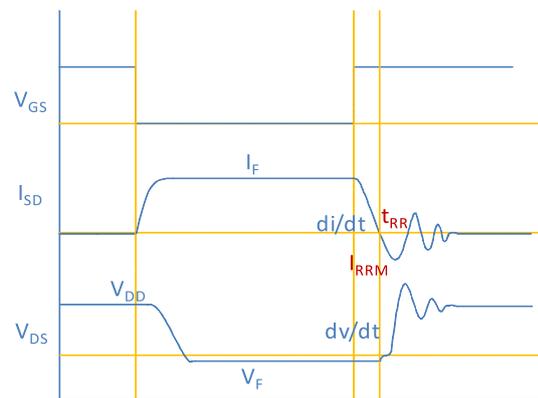
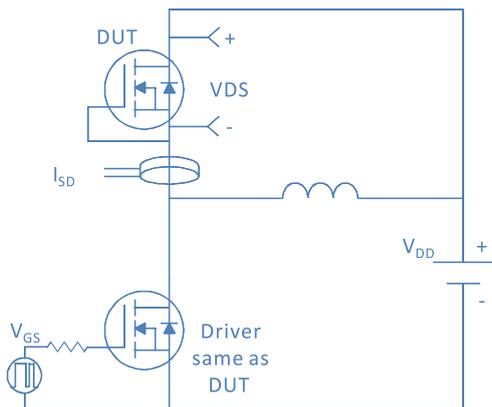
**Gate Charge Test**



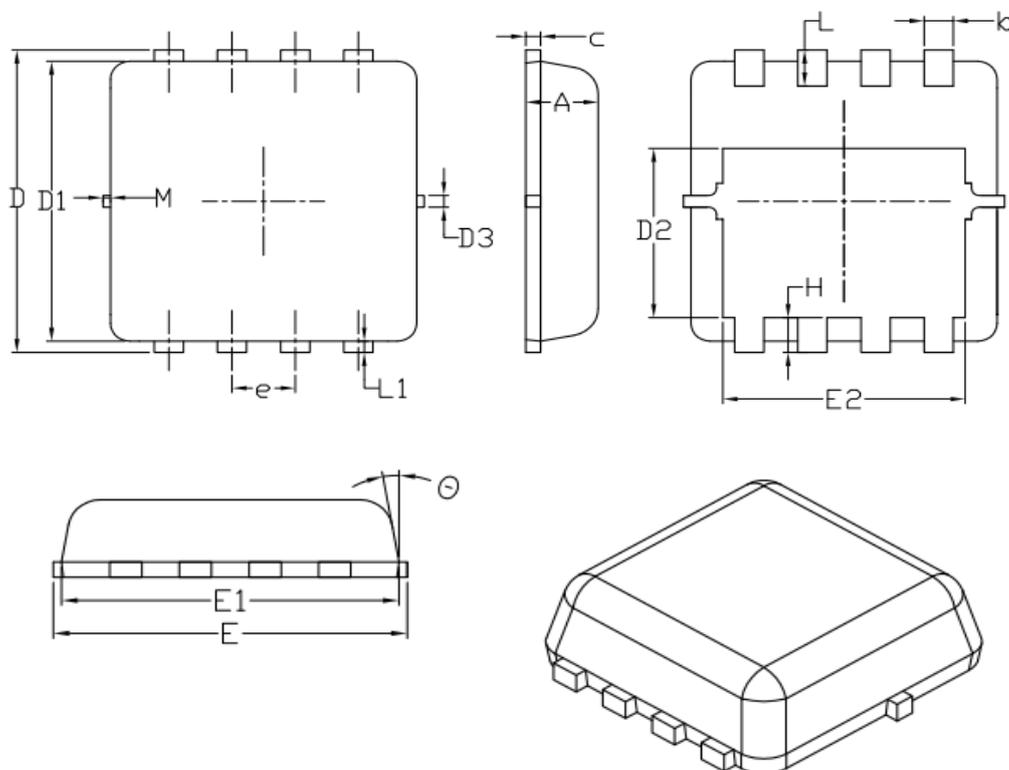
**Uclamped Inductive Switching (UIS) Test**



**Diode Recovery Test**



DFN3.3\*3.3\_P, 8 leads



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.00	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			