

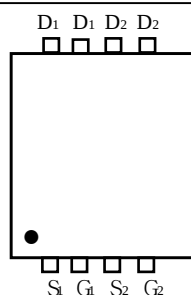
Dual N-Channel High Density Trench MOSFET

FEATURES

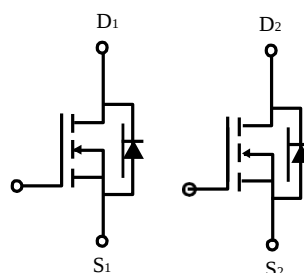
- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

PRODUCT SUMMARY

V (BR) DSS	$R_{DS(on)}$	ID
60V	7m Ω	32A



PDFN5x6



PARAMETERS TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source voltage		VGS	± 20	V
Continuous Drain current	TC = 25°C	ID	32	A
	TC = 100 °C		20	
Pulsed Drain Current ¹		IDM	100	
Avalanche Current		IAS	18	
Avalanche Energy	L=0.5mH	EAS	56	mJ
Power Dissipation	TC = 25 °C	PD		W
	TC = 100 °C		17	
Operating junction & Storage Temperature Range		Ts Tstg	-55 to 150	°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R θ Jc		3	°C /W
Junction-to-Ambient	R θ JA		40	°C /W

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage Gate	V(BR)DSS	VGS=0V,ID=250μA	30			V
Threshold Voltage	VGS(th)	VDS=VGS,ID=250μA	1	1.6	2.5	
Gate-Body Leakage	IGSS	VDS=0V,VGS=± 2 0V			±100	nA
Zero Gate Voltage Dain Current	IDSS	VDS=48V,VGS=0 V			1	μA
		VDS=20V,VGS=0V,TJ=125 °C			30	
Drain-Source On- State Resistance ¹	RDS(ON)	VGS=4.5V,ID=15A		11	16	mΩ
		VGS=10V,ID=20A		7	12	
Forward Trans conductance ¹	gfs	VDS=5V,ID=16A		12		S

DYNAMIC						
Input Capacitance Output	Ciss	VGS=0V, VDS=15V, f=1MHZ		1480		pF
Capacitance	Coss			276		
Reverse Transfer Capacitance Gate	Crss			31		
Resistance	RG	VGS=0V, f=1MHZ		3.5		Ω
Total Gate Charge ²	Qg(vgs=10V)	VDS=30V (BR)DSS, ID = 20A		15.5		nC
	Qg(vgs=4.5V)			12.8		
Gate Source Charge ²	QgS(VGS=10V)			8.5		
	QgS(VGS=4.5V)			6.7		
Gate-Drain Charge ²	Qgd(VGS=10V)			4.7		
	Qgd(VGS=4.5V)			3.2		
Tum-On Delay Time ²	td(on)	VDS=30V, RL=1.5Ω ID=20A, VGS=10V. RGS=6Ω		1.6		nS
Rise Time ²	tr			17		
Tum-Off Delay Time ²	td(off)			33		
Fall Time ²	tr			10.5		

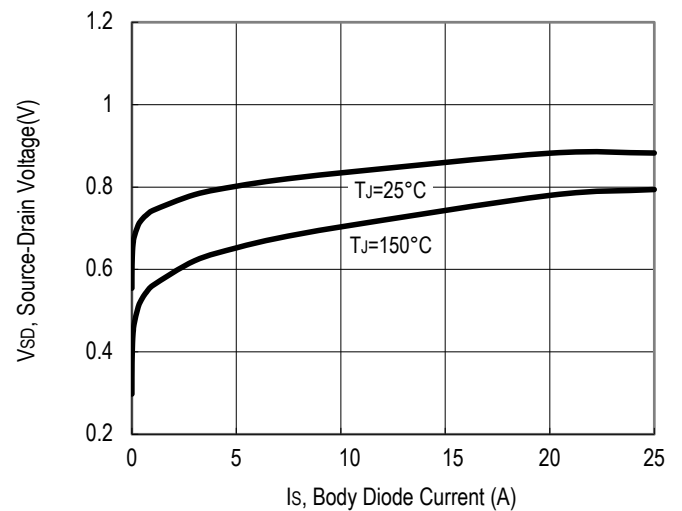
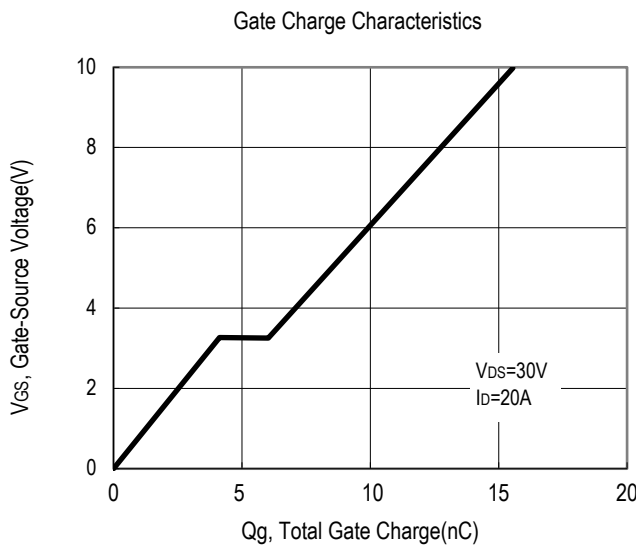
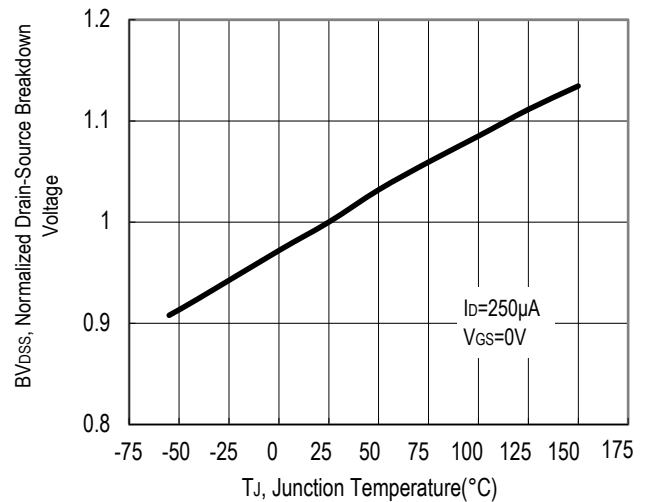
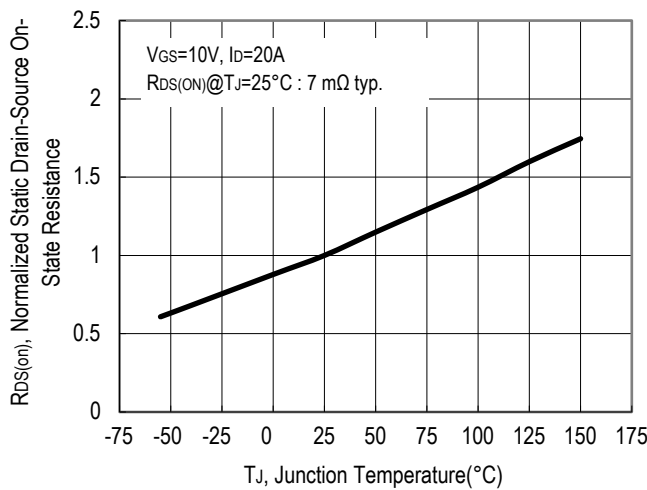
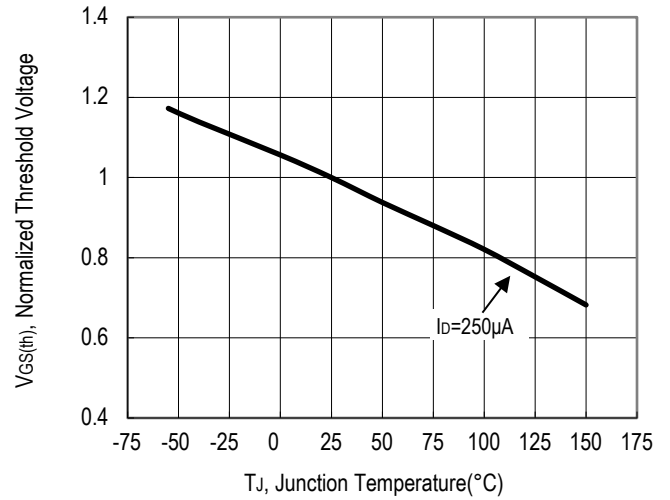
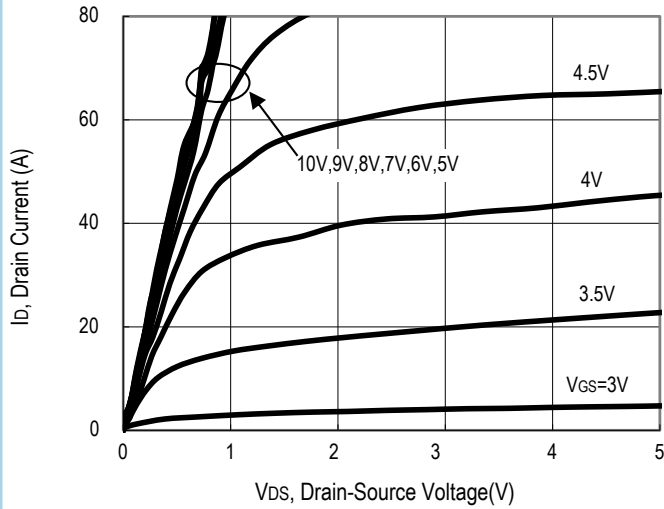
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS(TJ=25°C)

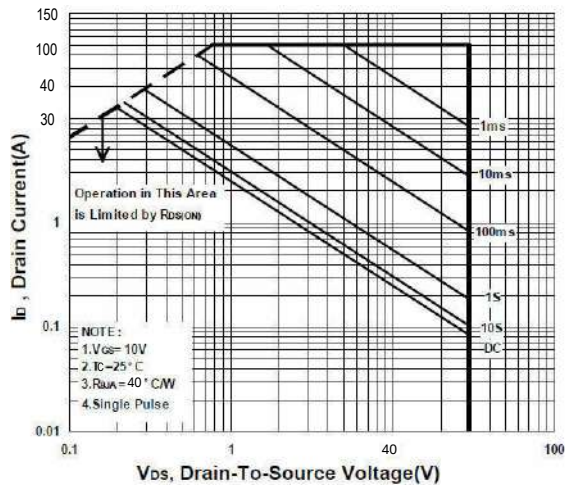
Continuous Current	IS			24		A
Forward Voltage ¹	VSD	IF=IS, VGS=0V		0.75	1.1	V
Reverse Recovery Time	Trr	IF=20V, dIf/dt=100A/μs		24		nS
Reverse Recovery Charge	Qrr			16		nC

Note

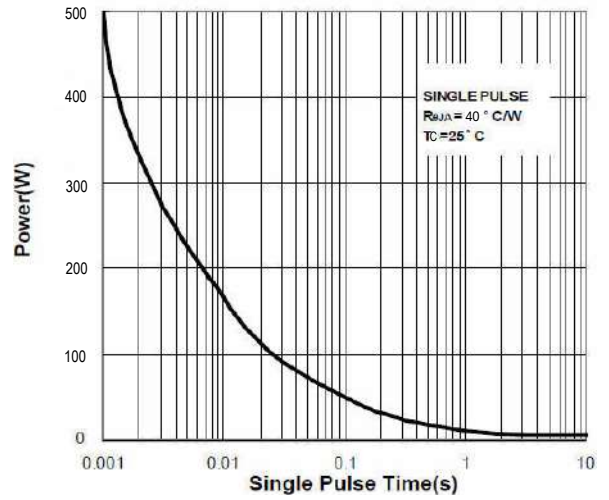
b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .

c. Independent of operating production testing .





Safe Operating Area



Single Pulse Maximum Power Dissipation

Transient Thermal Response Curves

