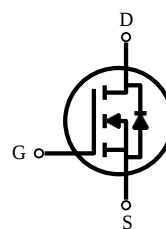
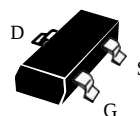


N-Channel High Density Trench MOSFET

FEATURES

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

SOT-323



PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m-ohm) Max
20V	3.3	65 @ $V_{GS} = 4.5V$
	2.0	90 @ $V_{GS} = 2.5V$

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous ^a @ $T_A = 25\text{ }^{\circ}\text{C}$ -Pulse ^b	I_D	3.3	A
	I_{DM}	12	A
Drain-Source Diode Forward Current ^a	I_S	1	A
Maximum Power Dissipation ^a	P_D	1.25	W
		0.75	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to 150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R_{thJA}	100	$^{\circ}\text{C/W}$
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Note

a. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

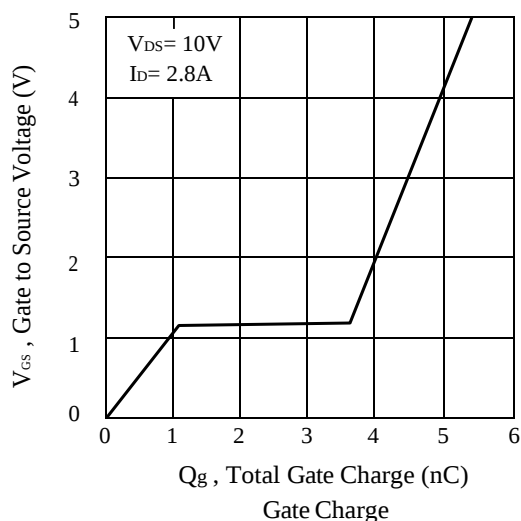
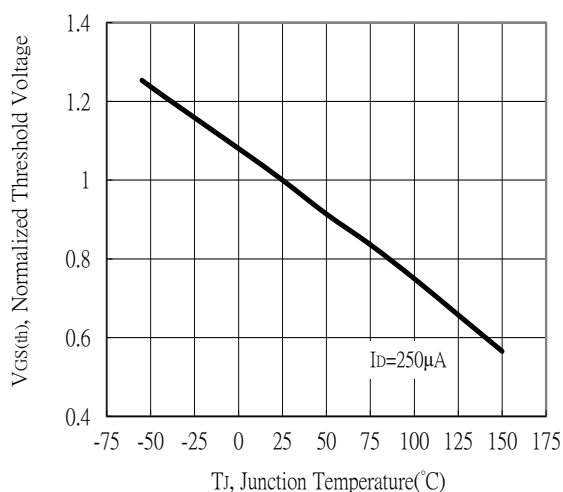
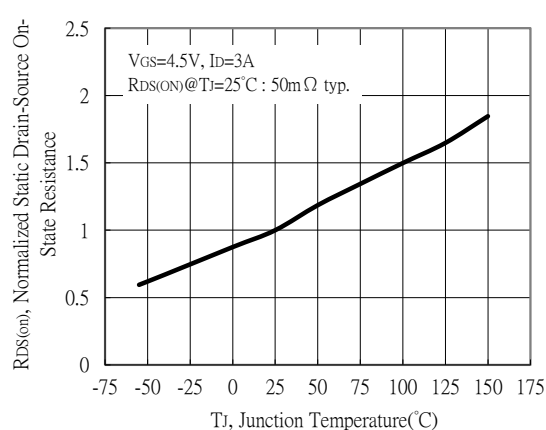
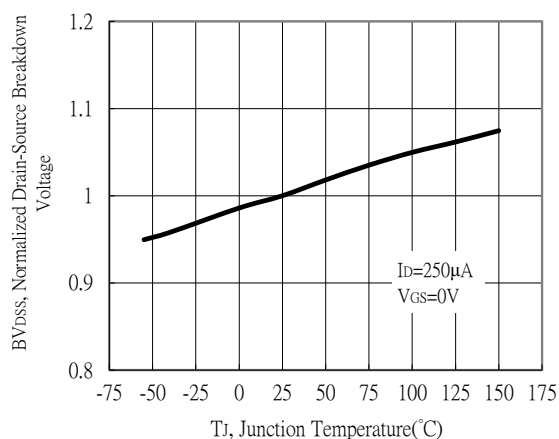
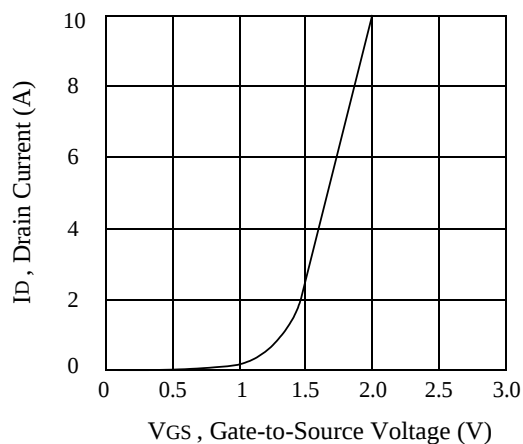
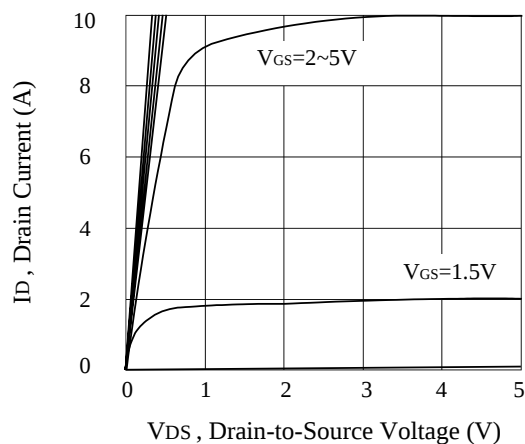
b. Pulse width limited by maximum junction temperature.

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V , I _D = 250uA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V , V _{GS} = 0V			1	uA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±8V , V _{DS} = 0V			±10	uA
ON CHARACTERISTICS ^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	0.5	0.7	1	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 4.5V , I _D = 2.8A		50	65	m-ohm
		V _{GS} = 2.5V , I _D = 2.0A		65	90	
Forward Transconductance	g _{fs}	V _{DS} = 5V , I _D = 4A		7		S
DRAIN-SOURCE DIODE CHARACTERISTICS ^b						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V , I _S = 1.7A			1.2	V
DYNAMIC CHARACTERISTICS ^c						
Input Capacitance	C _{ISS}	V _{DS} = 6V , V _{GS} = 0V f = 1.0MHz		280		pF
Output Capacitance	C _{OSS}			45		pF
Reverse Transfer Capacitance	C _{RSS}			40		pF
SWITCHING CHARACTERISTICS ^c						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 6V , I _D = 1A V _{GEN} = 4.5V R _L = 6 ohm R _{GEN} = 6 ohm		3.5		ns
Rise Time	t _r			19.5		ns
Turn-Off Delay Time	t _{D(OFF)}			22.8		ns
Fall Time	t _f			24.2		ns
Total Gate Charge	Q _g	V _{DS} = 10V		5.3		nC
Gate-Source Charge	Q _{gs}	I _D = 2.8A		0.8		nC
Gate-Drain Charge	Q _{gd}	V _{GS} = 4.5V		1.5		nC

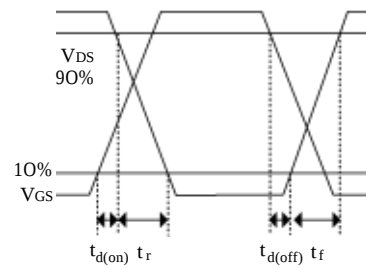
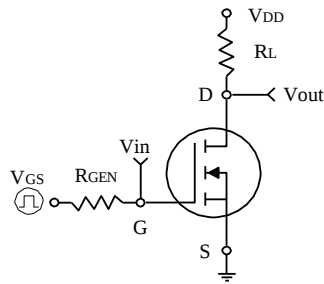
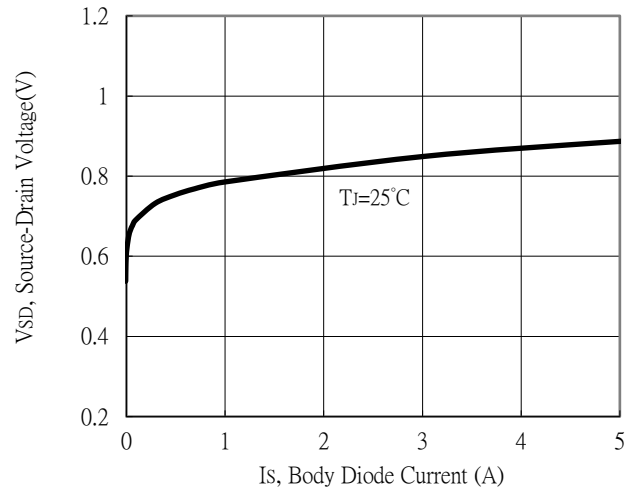
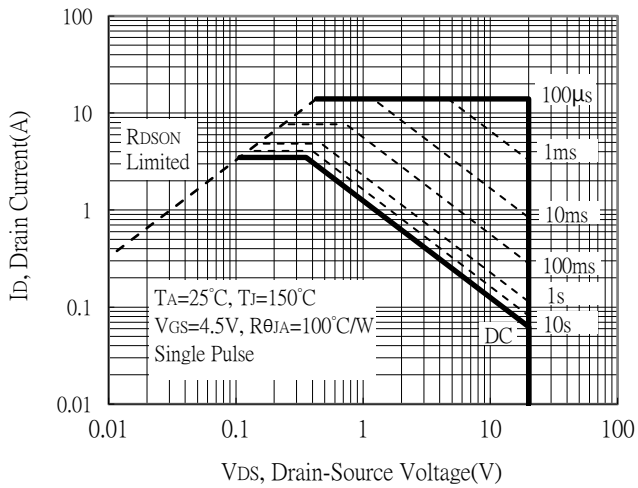
Note

b. Pulse Test Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

c. Guaranteed by design, not subject to production testing.



Maximum Safe Operating Area



Switching Test Circuit and Switching Waveforms

