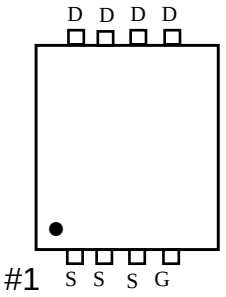
# N-Channel High Density Trench MOSFET

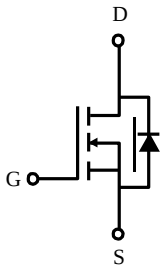
## FEATURES

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

PDFN3x3




| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{(BR)DSS}$ | $R_{DS(ON)}$ | $I_D$ |
| 100V | 16mΩ | 53A |




## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C unless otherwise noted)

| PARAME TERS TEST CONDITIONS | | SYMBOL | LIMITS | UNITS |
|---|---|---|---|---|
| Gata-Source voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain current | $T_C$ = 25℃ | $I_D$ | 27 | A |
| | $T_C$ =100℃ | | 17 | |
| Puised Drain Current[1] | | $I_{DM}$ | 80 | |
| Avalanche Current | | $I_{AS}$ | 30 | |
| Avalanche Energy | L=0.1mH | $E_{AS}$ | 45 | mJ |
| Power Dissipation | $T_C$ = 25 ℃ | $P_D$ | 27.7 | W |
| | $T_C$ =100℃ | | 10.5 | |
| Operaing junction & Storege Temperature Range | | Ts,Tstg | -55 to 150 | ℃ |

## THERMAL CHARACTERISTICS

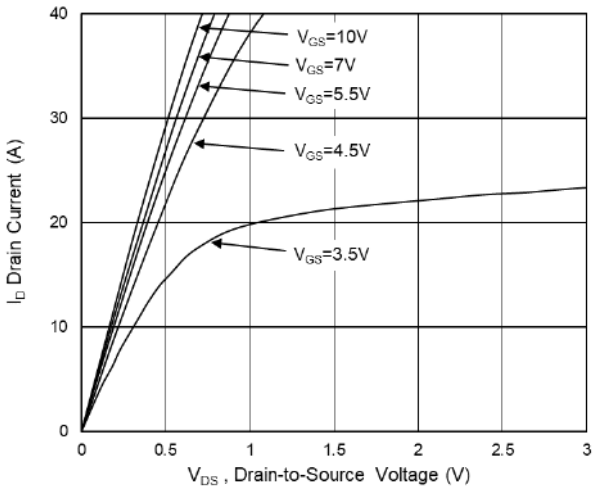
| THERMAL RESISTANCE | SYMBOL | TYPICAL | MAXIMUM | UNITS |
|---|---|---|---|---|
| Junction-to-Case | RθJc | | 4.5 | ℃/W |
| Junction-to-Ambient | RθJA | | 55 | ℃/W |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C unless otherwise noted)

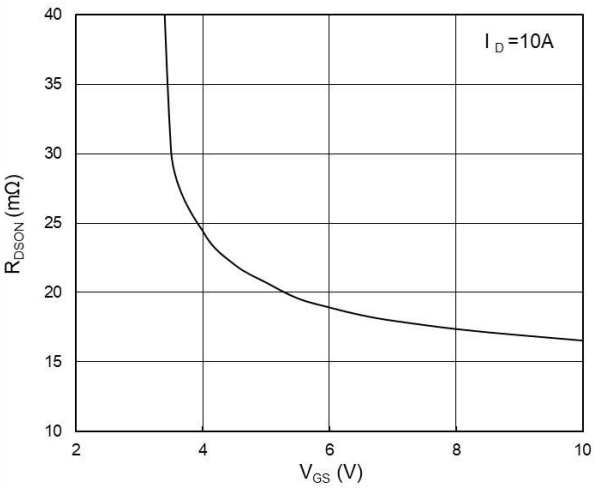
| PARAMETER | SYMBOL | TEST CONDITIONS | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC** | | | | | | |
| Drain-Source Breakdown Voltege | $V_{(BR)DSS}$ | $V_{GS}$=0V,$I_D$=250μA | 100 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.2 | 1.8 | 2.2 | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$=0V,$V_{GS}$=± 20V | | | ±100 | nA |
| Zero Gate Voltage Dain Current | $I_{DSS}$ | $V_{DS}$=80V,$V_{GS}$=0 V | | | 1 | μA |
| | | $V_{DS}$=80V,$V_{GS}$=0V,$T_J$=55℃ | | | 5 | μA |
| Drain-Source On- State Resistance[1] | $R_{DS(ON)}$ | $_{GS}$=10V,$I_D$=10A | | 16 | 20 | mΩ |
| | | $V_{GS}$=4.5V,$I_D$=10A | | 21 | 30 | mΩ |
| Forward Trans conductance[1] | $g_{fs}$ | $V_{DS}$=5V,$I_D$=10A | | 12 | | S |
| **DYNAMIC** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$=0V,$V_{DS}$=50V,f=1MHz | | 849 | | pF |
| Output Capacitance | $C_{oss}$ | | | 185 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 8 | | pF |
| Gate Resistance | $R_G$ | $V_{GS}$=0V,f=1MHz | | 1 | | Ω |
| Total Gate Charge[2] | $Q_{g(vgs=10V)}$ | $V_{DS}$=50V $_{(BR)DSS}$, $I_D$ = 20A | | 17.9 | | nC |
| | $Q_{g(vgs=4.5V)}$ | | | 6.7 | | nC |
| Gate Source Charge[2] | $Q_{gS(VGS=10V)}$ | | | 2.8 | | nC |
| Gate-Drain Charge[2] | $Q_{gd(VGS=10V)}$ | | | 5.2 | | nC |
| Tum-On Delay Time[2] | $t_{d(on)}$ | $V_{DS}$=30V, $I_D$=1A,$V_{GS}$=10V.$R_{GS}$=6Ω | | 13 | | nS |
| Rise Time[2] | $t_r$ | | | 6 | | nS |
| Tum-Off Delay Time[2] | $t_{d(off)}$ | | | 30 | | nS |
| Fall Time[2] | $t_r$ | | | 29 | | nS |
| **SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS($T_J$=25℃)** | | | | | | |
| Continuous Current | $I_S$ | | | | 27 | A |
| Forward Voltage[1] | $V_{SD}$ | $I_F$=$I_S$,$V_{GS}$=0V | | 0.75 | 1.2 | V |
| Reverse Recovery Time | $T_{rr}$ | $I_F$=10A,$d_{1f}$/$d_t$=100A/μs | | 28 | | nS |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$=10A,$d_{1f}$/$d_t$=100A/μs | | 23 | | nC |

Note
b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .
c. Independent of operating production testing .

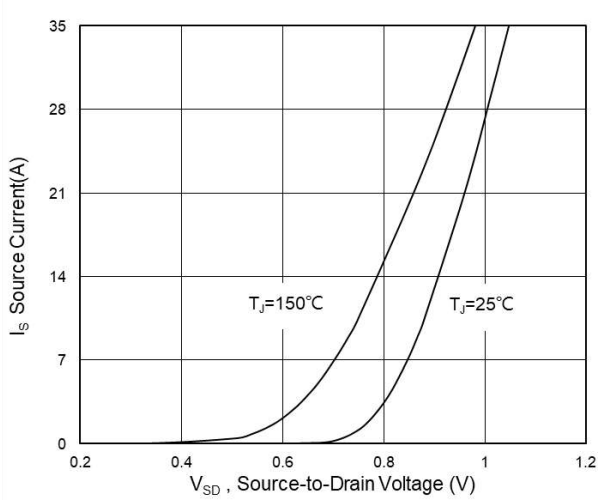
## Typical Characteristics



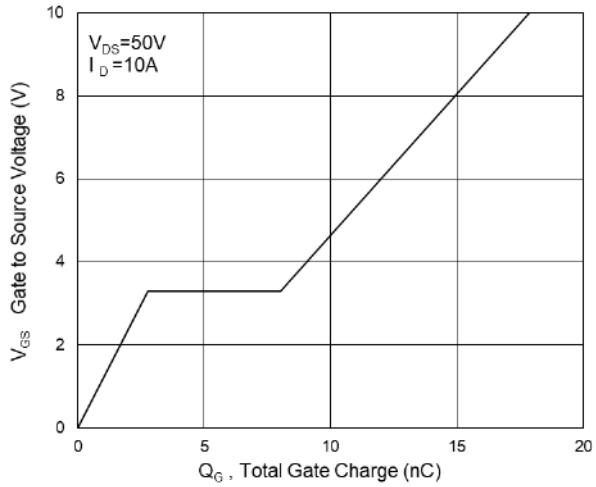

**Typical Output Characteristics**



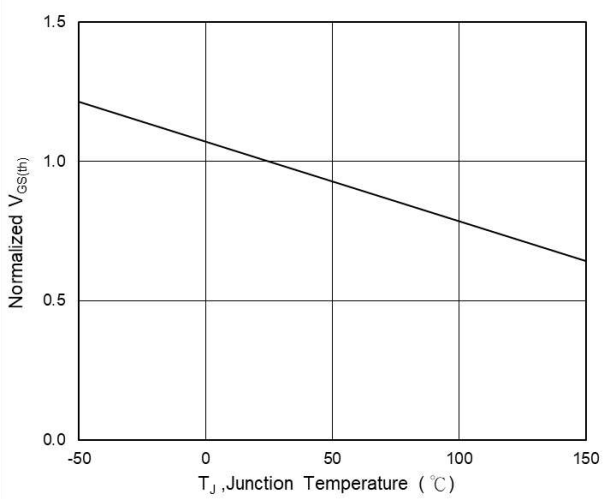

**On -Resistance vs G-S Voltage**



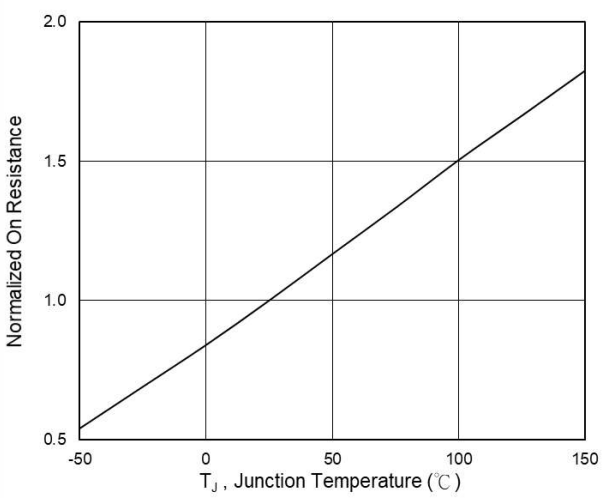

**Source Drain Forward Characteristics**



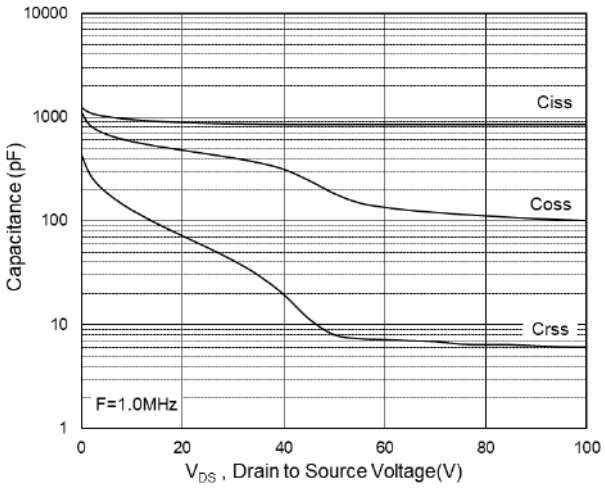

**Gate-Charge Characteristics**



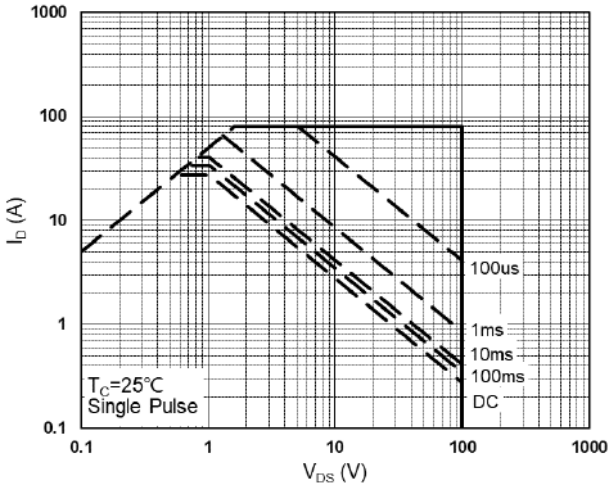

**Normalized $V_{GS(th)}$ vs $T_J$**



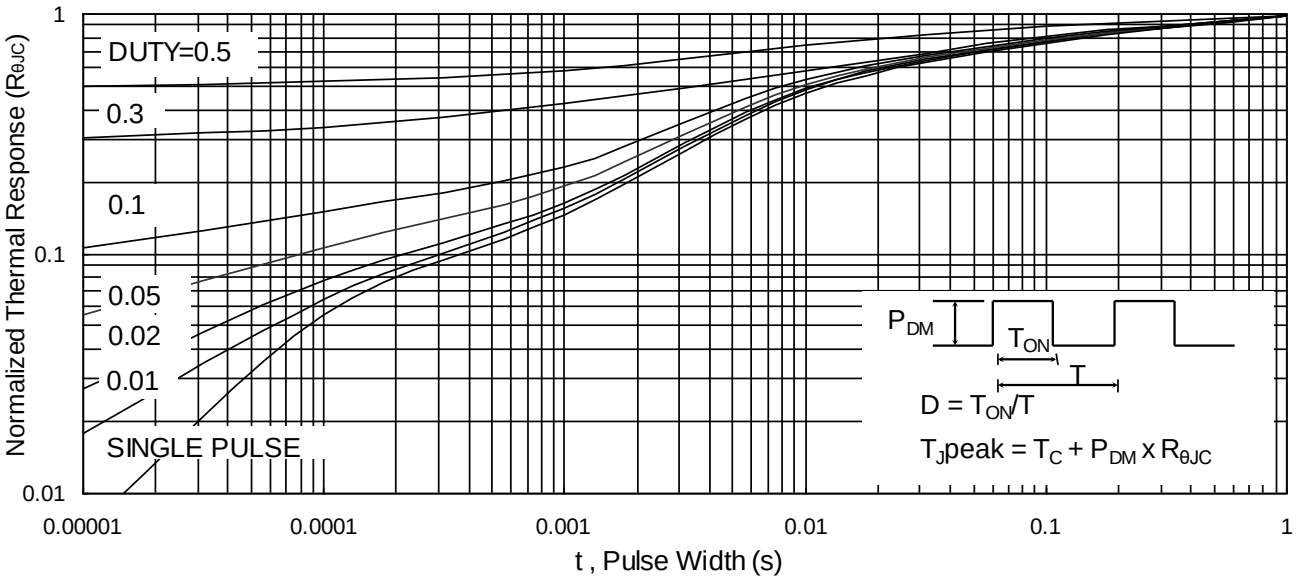

**Normalized $R_{DSON}$ vs $T_J$**




**Capacitance**




**Safe Operating Area**




**Normalized Maximum Transient Thermal Impedance**