

## P-Channel High Density Trench MOSFET

### Features:

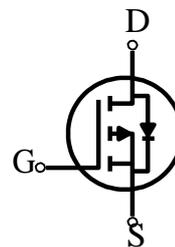
- Super high dense cell trench design for low  $R_{DS(on)}$ .
- Rugged and reliable.
- Surface Mount package.

SOT-23



### PRODUCT SUMMARY

VDSS	ID	RDS(on) (m-ohm) Max
-20V	-3.5 A	50 @ VGS = 4.5V
	-1.2 A	65 @ VGS = 2.5V



### DEVICE MARKING

KL2305 = 2305 / A5SHB

### ABSOLUTE MAXIMUM RATINGS (TA = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	-20	V
Gate-Source Voltage	VGS	12	V
Drain Current-Continuous <sup>a</sup> @ TA= 25 °C -Pulse <sup>b</sup>	ID	-4	A
	IDM	-15	A
Maximum Power Dissipation <sup>a</sup>	PD	1.25	W
Operating Junction and Storage Temperature Range	TJ, Tsig	- 55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	RthJA	100	°C/W
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Note

a. Surface Mounted on FR4 Board , t ≤ 10sec .

b. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V , I <sub>D</sub> = -250uA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30V , V <sub>GS</sub> = 0V			-1	uA
Gate-Body Leakage Current, Forward	I <sub>GSSF</sub>	V <sub>GS</sub> = 12V , V <sub>DS</sub> = 0V			100	nA
Gate Body Leakage Current, Reverse	I <sub>GSSR</sub>	V <sub>GS</sub> = -12V, V <sub>DS</sub> = 0V			-100	nA
<b>ON CHARACTERISTICS<sup>c</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250uA	-0.7		-1.3	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V , I <sub>D</sub> = 4A		40	45	m Ω
		V <sub>GS</sub> = -4.5V , I <sub>D</sub> = -3.5A		45	50	m Ω
		V <sub>GS</sub> = -2.5V , I <sub>D</sub> = -1.2A		60	65	m Ω
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -10V, I <sub>D</sub> = -4A		5		S
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -15V , V <sub>GS</sub> = 0V f = 1.0MHz		900		pF
Output Capacitance	C <sub>OSS</sub>			155		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			205		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = -15V , I <sub>D</sub> = 4A V <sub>GEN</sub> = -10V R <sub>GEN</sub> = 6 ohm		9	20	ns
Rise Time	t <sub>r</sub>			4	10	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			42	85	ns
Fall Time	t <sub>f</sub>			5	10	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15V I <sub>D</sub> = -4A V <sub>GS</sub> = -4.5V		8.4	11	nC
Gate-Source Charge	Q <sub>gs</sub>			2.4		nC
Gate-Drain Charge	Q <sub>gd</sub>			1.5		nC
<b>Drain-Source Diode Characteristics and Maximun Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	I <sub>S</sub>				-4	A
Drain-Source Diode Forward Voltage <sup>c</sup>	V <sub>S</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A			-1	V

Note

b. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2% .

c. Guaranteed by design , not subject to production testing .

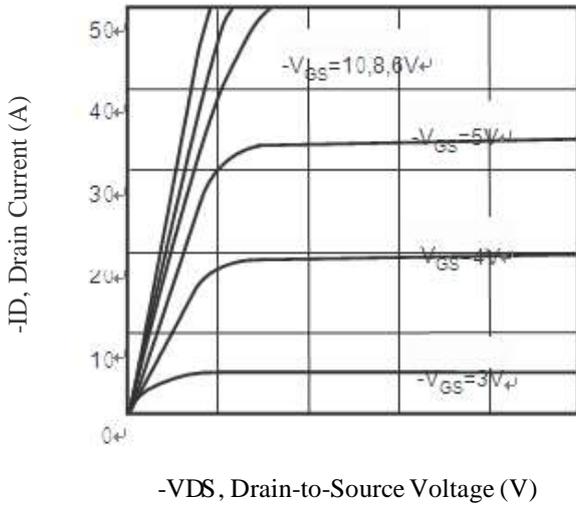


Figure 1. Output Characteristics

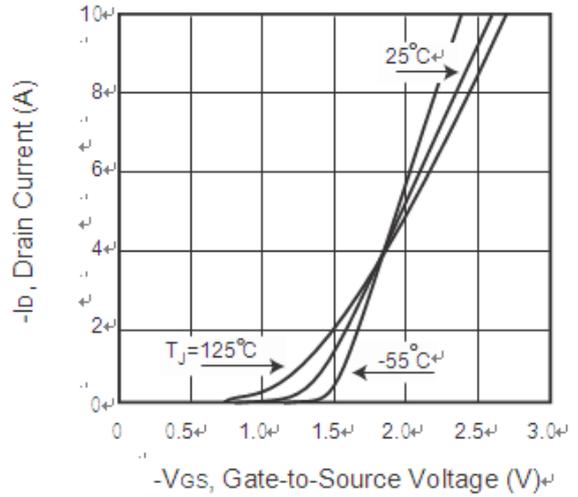


Figure 2. Transfer Characteristics

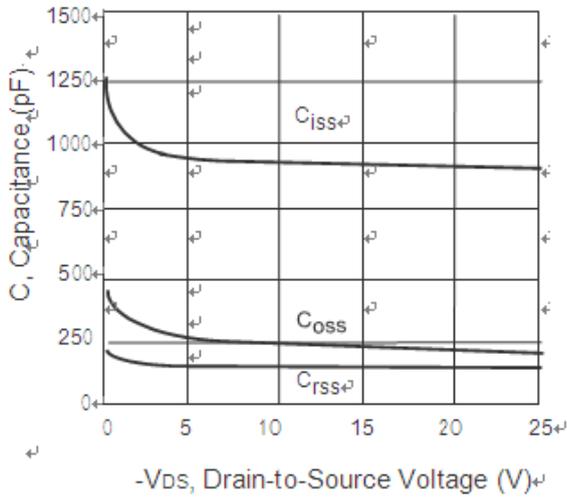


Figure 3. Capacitance

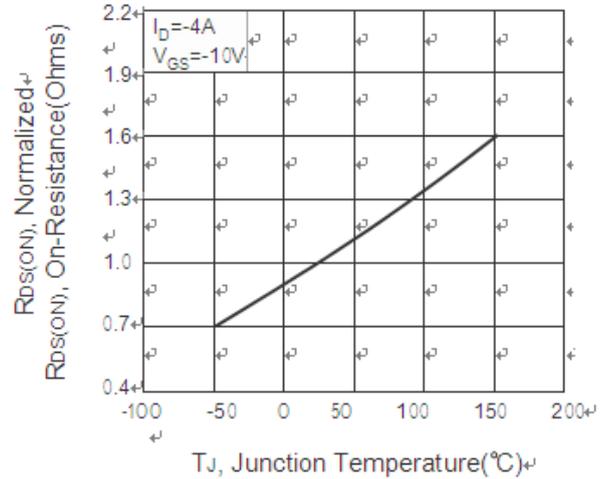


Figure 4. On-Resistance Variation with Temperature

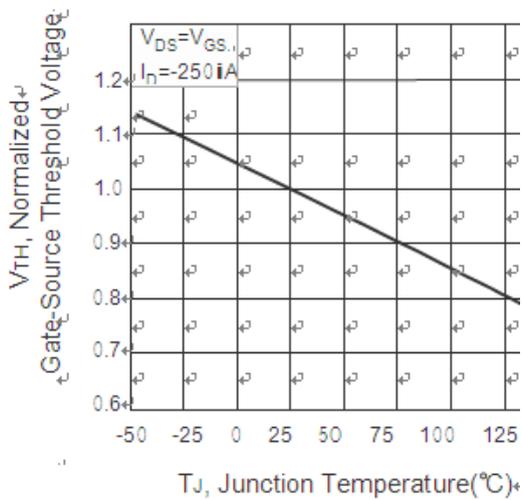


Figure 5. Gate Threshold Variation with Temperature

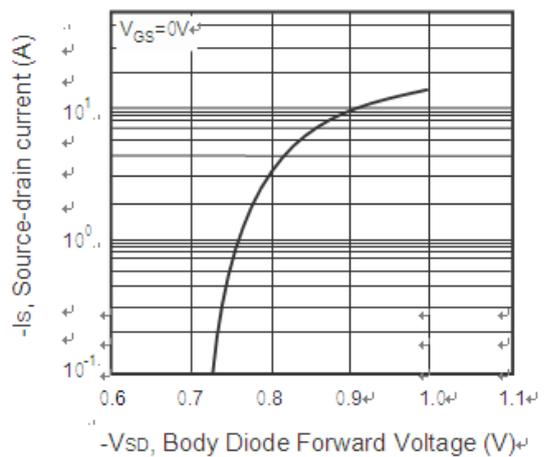


Figure 6. Body Diode Forward Voltage Variation with Source Current

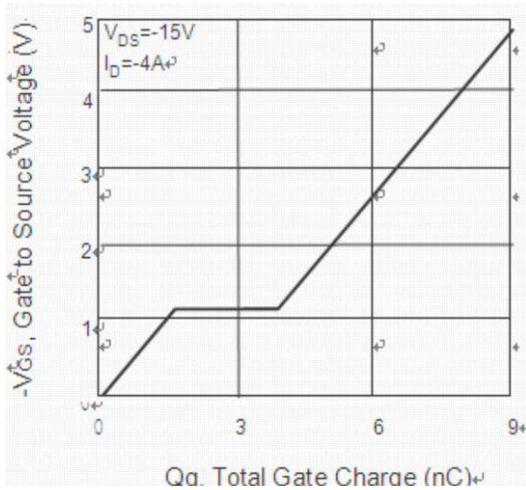


Figure 7. Gate Charge

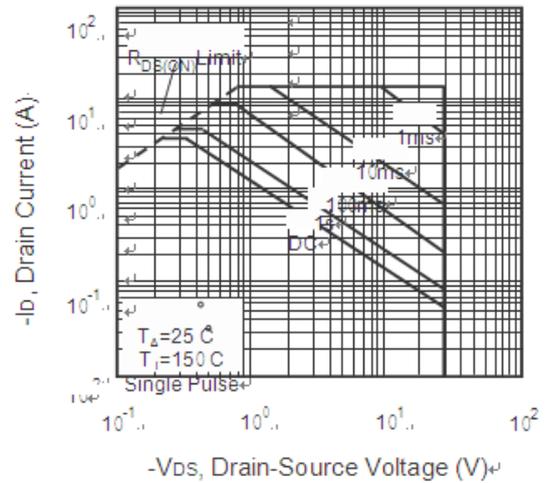


Figure 8. Maximum Safe Operating Area

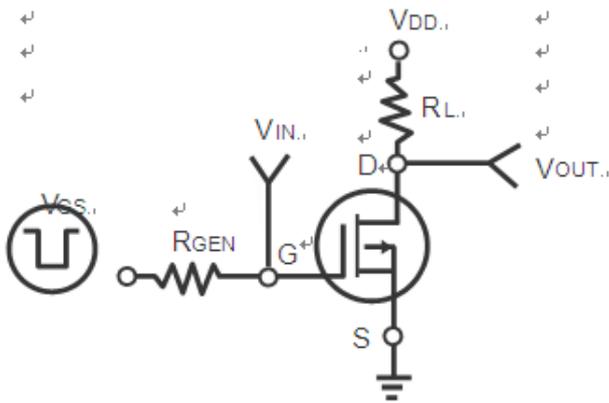


Figure 9. Switching Test Circuit

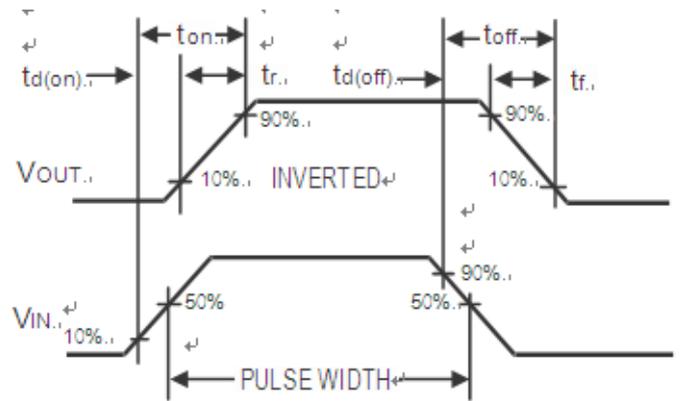


Figure 10. Switching Waveforms

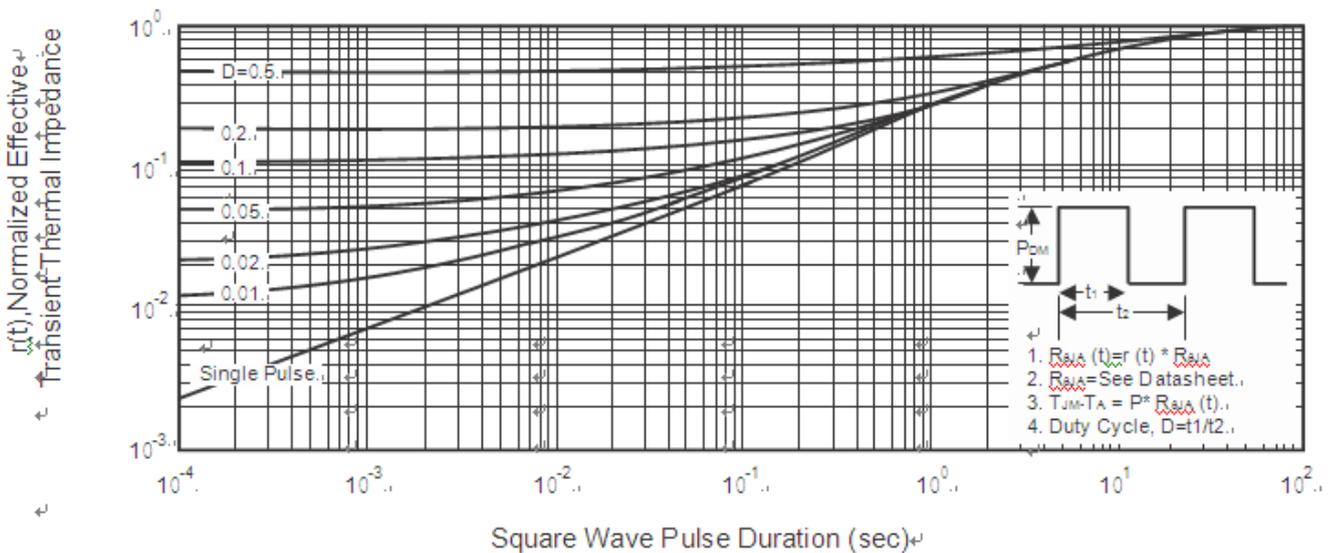
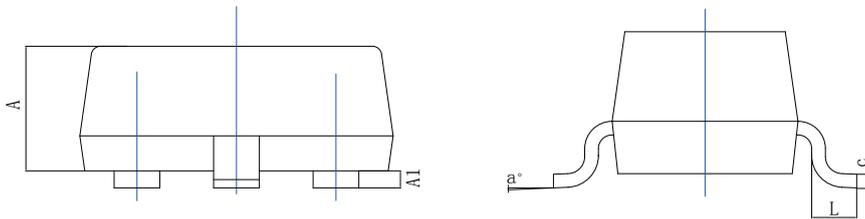


Figure 11. Normalized Thermal Transient Impedance Curve

**SOT-23 Outline Dimensions**

Unit:mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.35
A1	0.04	0.07	0.15
b	0.30	0.40	0.50
c	0.08	--	0.21
D	2.72	2.92	3.12
E	2.10	2.33	2.64
E1	1.10	1.30	1.50
e	0.95BSC		
L	0.20	--	0.60
a°	0°	--	8°

