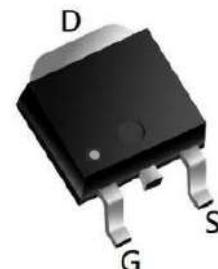


N-Ch 60V Fast Switching MOSFETs

Features

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

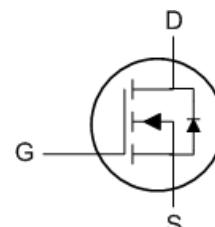
TO252 Pin Configuration



Description

The KJD6032A is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The KJD6032A meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.



Product Summary

BVDSS	RDSON	ID
60V	8.5mΩ	75A

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	60	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	75	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	47	A
I _{DM}	Pulsed Drain Current ²	280	A
EAS	Single Pulse Avalanche Energy ³	80	mJ
I _{AS}	Avalanche Current	40	A
P _D @T _C =25°C	Total Power Dissipation ⁴	41	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-case ¹	---	1.4	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	60	---	---	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	7.1	8.5	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	2.2	---	4.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.2	---	Ω
Q_g	Total Gate Charge (10V)	$V_{\text{DS}}=30\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=18\text{A}$	---	57	---	nC
Q_{gs}	Gate-Source Charge		---	8.7	---	
Q_{gd}	Gate-Drain Charge		---	14	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=30\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_g=3.3\Omega$, $I_D=20\text{A}$	---	16.2	---	ns
T_r	Rise Time		---	41.2	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	56.4	---	
T_f	Fall Time		---	16.2	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=30\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	3307	---	pF
C_{oss}	Output Capacitance		---	201	---	
C_{rss}	Reverse Transfer Capacitance		---	151	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	75	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	22	---	nS
			---	72	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=40\text{A}$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

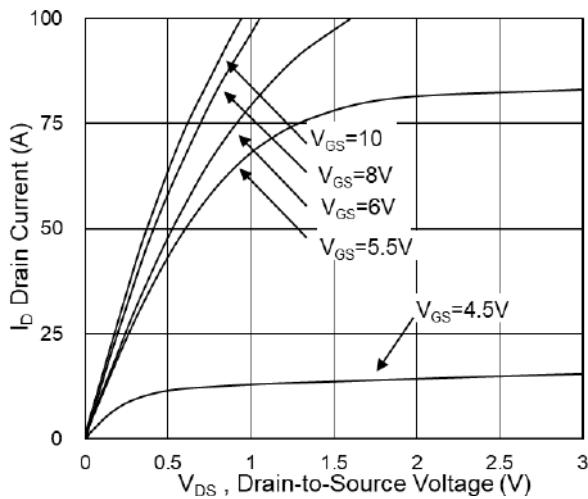


Fig.1 Typical Output Characteristics

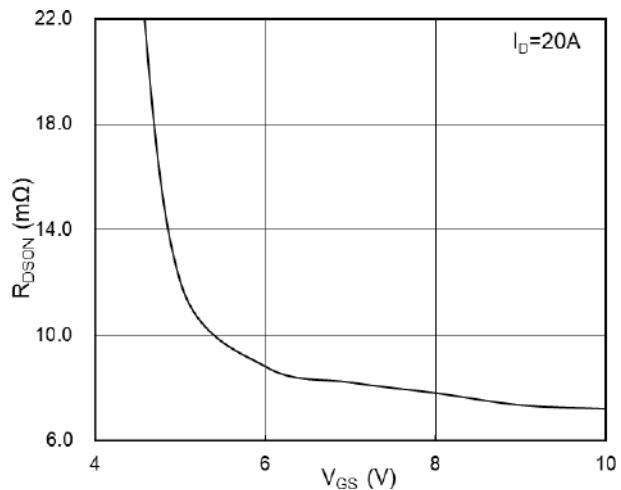


Fig.2 On-Resistance vs G-S Voltage

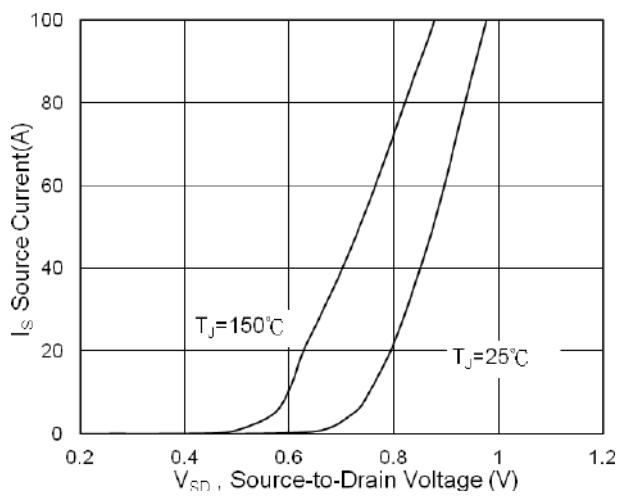


Fig.3 Source Drain Forward Characteristics

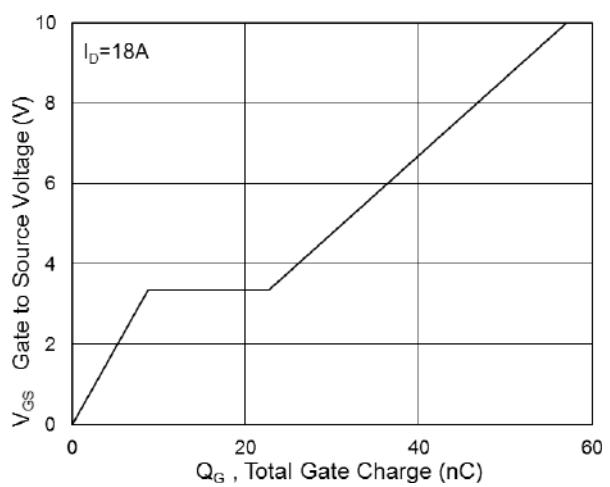


Fig.4 Gate-Charge Characteristics

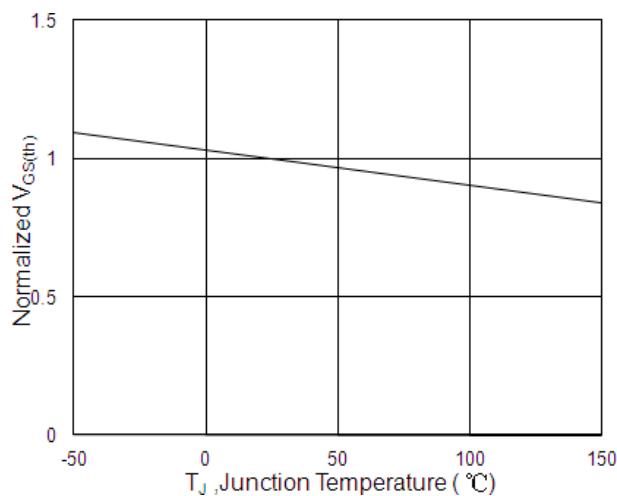


Fig.5 Normalized $V_{GS(th)}$ vs T_J

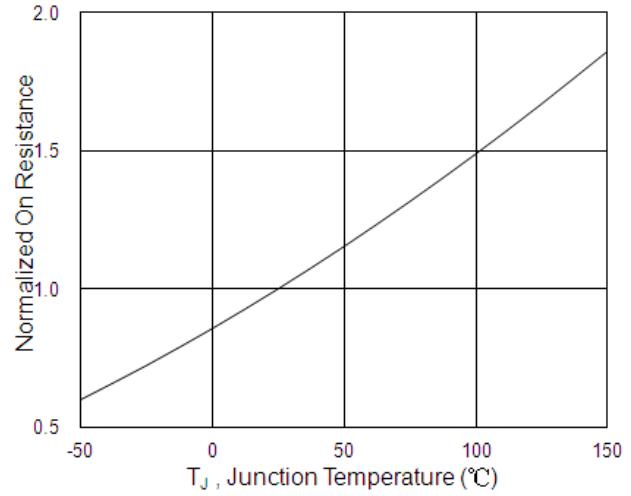


Fig.6 Normalized $R_{DS(on)}$ vs T_J

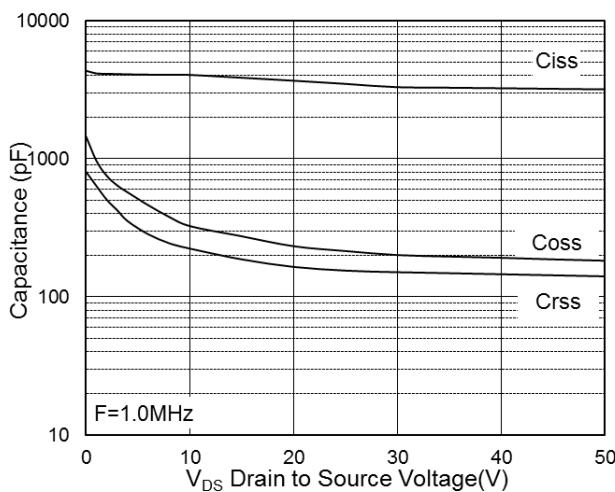


Fig.7 Capacitance

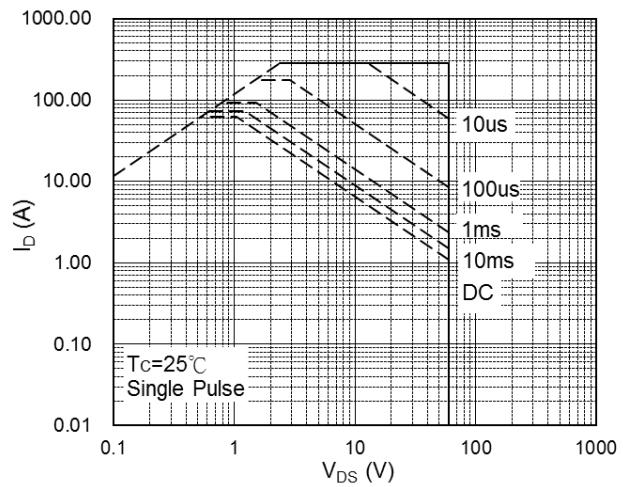


Fig.8 Safe Operating Area

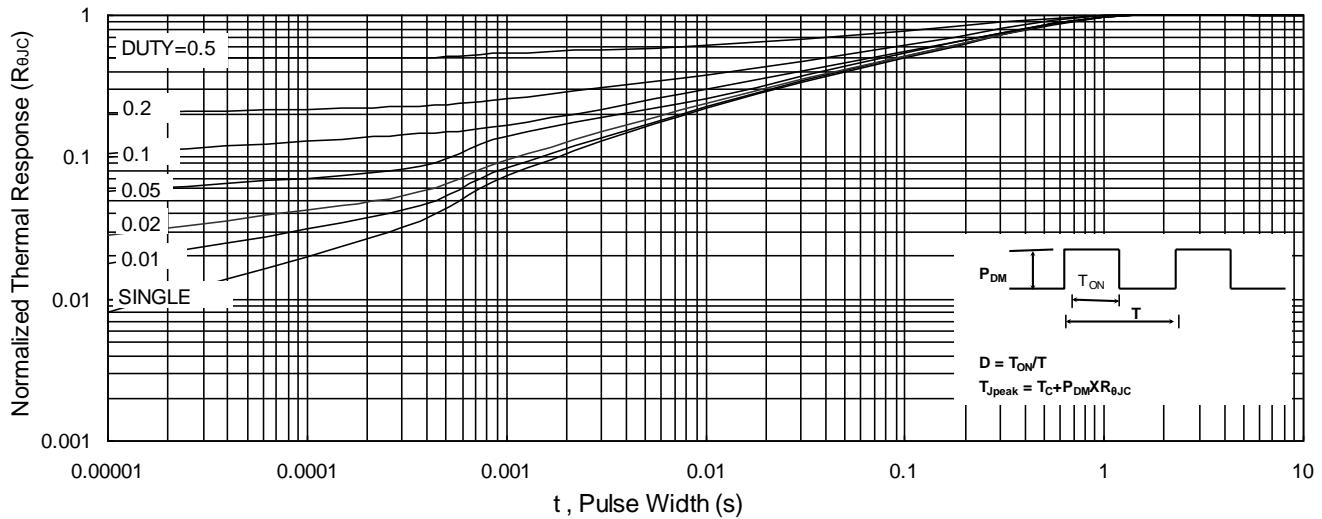


Fig.9 Normalized Maximum Transient Thermal Impedance

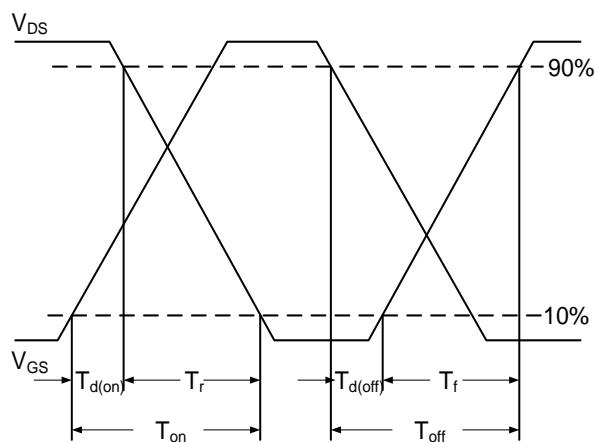


Fig.10 Switching Time Waveform

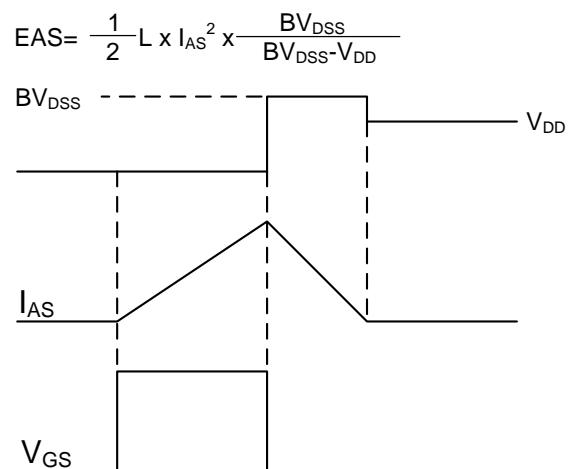


Fig.11 Unclamped Inductive Switching Waveform