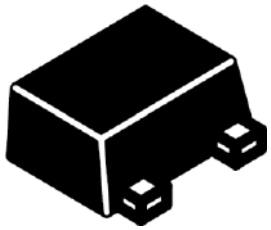
LOW CAPACITANCE TVS DIODE ARRAY

Features:

- 100 Watts Peak Pulse Power per Line (tp=8/20μs)
- Protects Two Lines
- Low Clamping Voltage
- Working Voltages : 5.3V
- Low Leakage Current
- IEC61000-4-2 (ESD) ±17kV (air), ±10kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ηs)
- IEC61000-4-5 (LIGHTING) 4A (8/20μs)

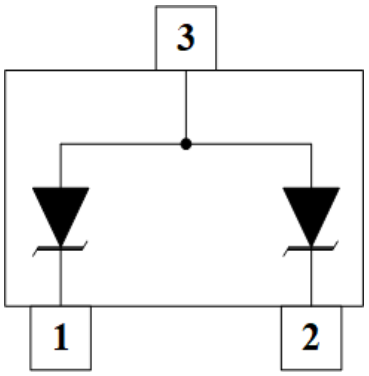
Dimensions SOT-723



Applications:

- Optical Modules
- USB Type-C
- V-By-One
- eSATA
- HDMI 1.4, HDMI1.4b and HDMI 2.0
- Display Port 1.2

Pin Configuration



Mechanical Characteristics

- SOT-723 Package
- Molding Compound Flammability Rating : UL 94V-O
- Weight 1.3 Millgrams (Approximate)
- Quantity Per Reel : 8,000pcs
- Reel Size : 7 inch
- Device Marking:M5

Absolute Maximum Ratings(Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Current (8/20μs)	Ppp	80	W
ESD per IEC 61000−4−2 (Air)	V_{ESD}	±17	Kv
ESD per IEC 61000−4−2 (Contact)		±10	
Operating Temperature Range	T_J	-40 to +125	℃
Storage Temperature Range	T_{STJ}	-55 to +150	℃

Electrical Characteristics(TA=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				5.3	V
Breakdown Voltage	V_{BR}	I_T = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5.3V			1	μA
Clamping Voltage	V_C	I_{PP} = 1A (8 x 20 μs pulse)			12	V
Clamping Voltage	V_C	I_{PP} = 4A (8 x 20 μs pulse)			20	V
Junction Capacitance	C_J	V_R = 0V, f = 1MHz		0.4		pF

TYPIC CHARACTERISTICS

Figure 1. 8 x 20μs Waveform

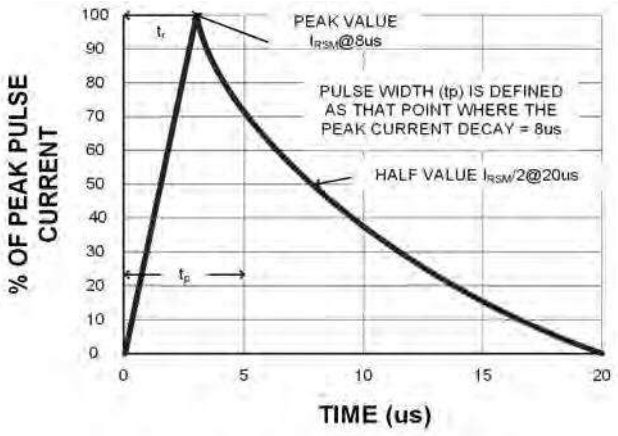


Figure 2. Power Derating Curve

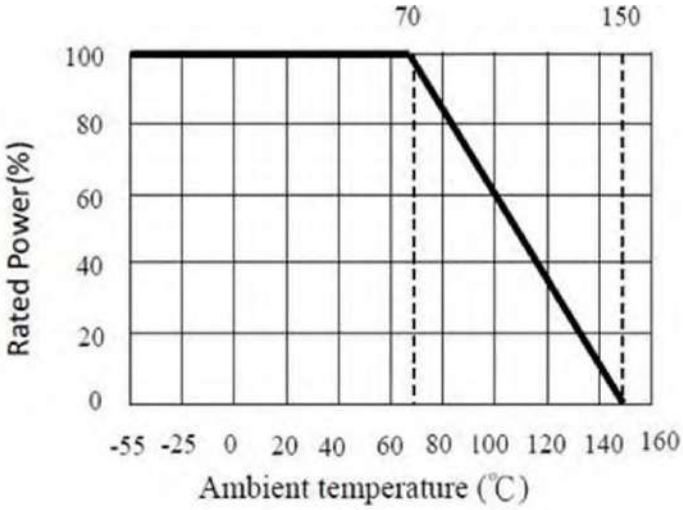
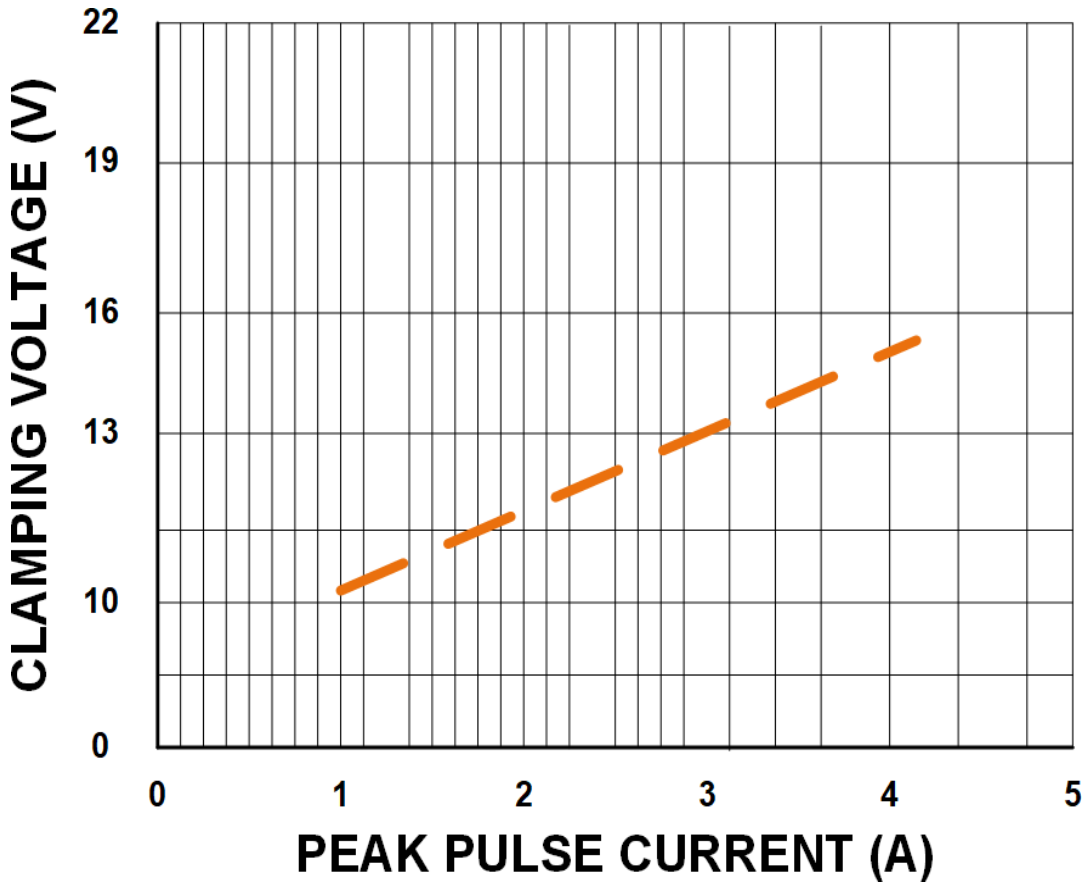


Figure 3. Clamping Voltage vs. Peak Pulse Current (TLP/1A, tp = 100ηs)



TYPIC CHARACTERISTICS

Figure 4. Typic Breakdown Voltage vs. Temperature

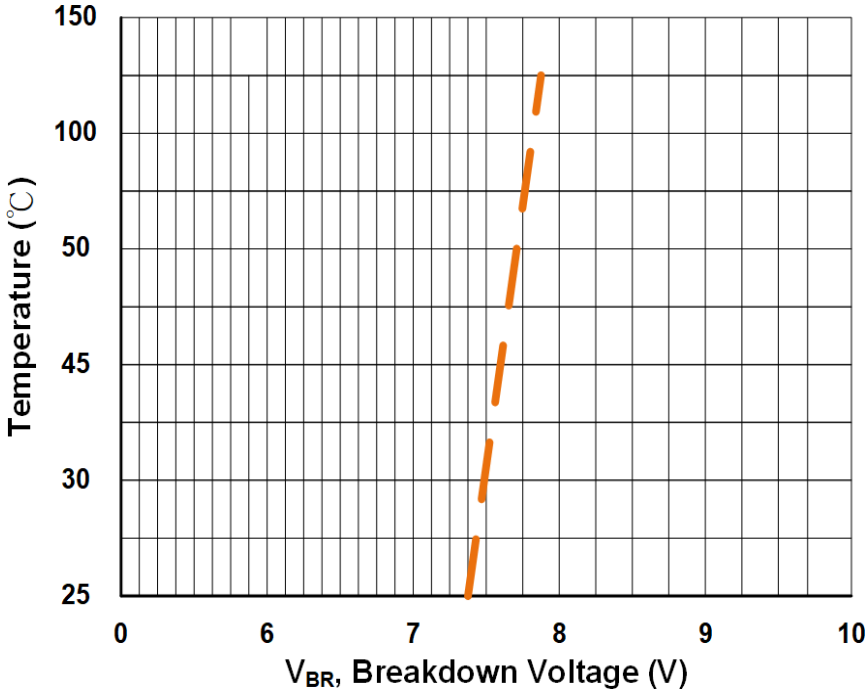


Figure 5. Typic Reverse Current vs. Temperature

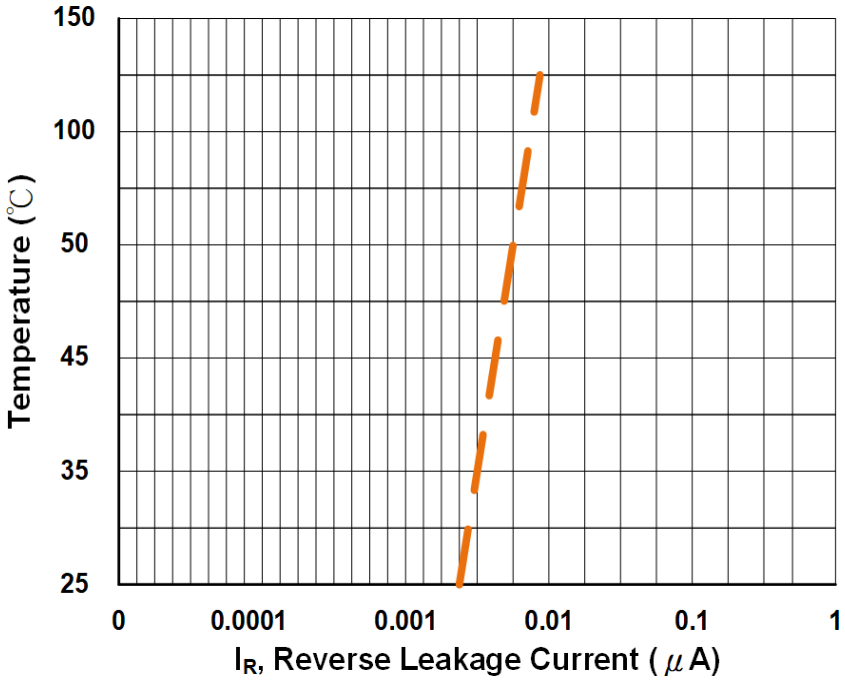
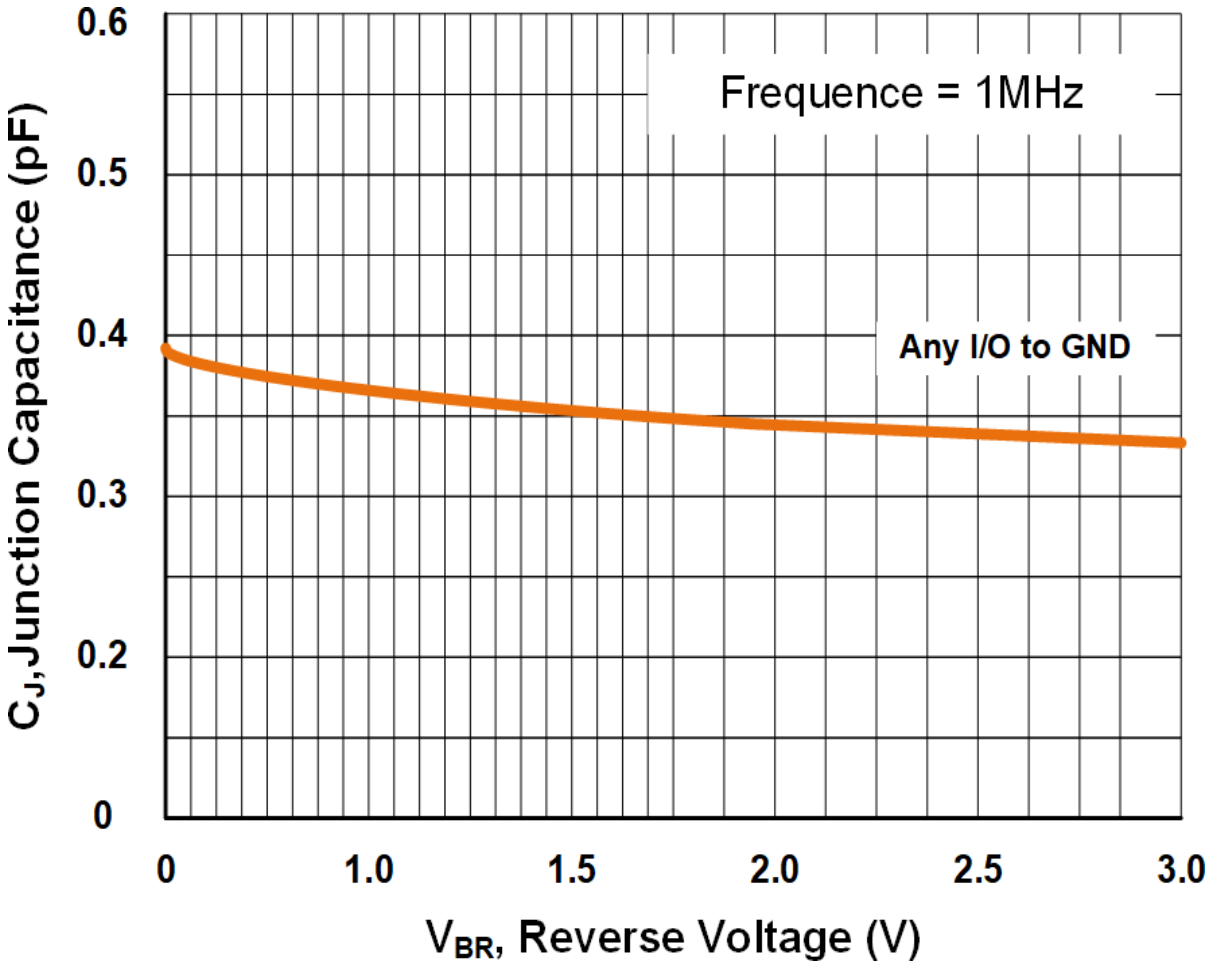


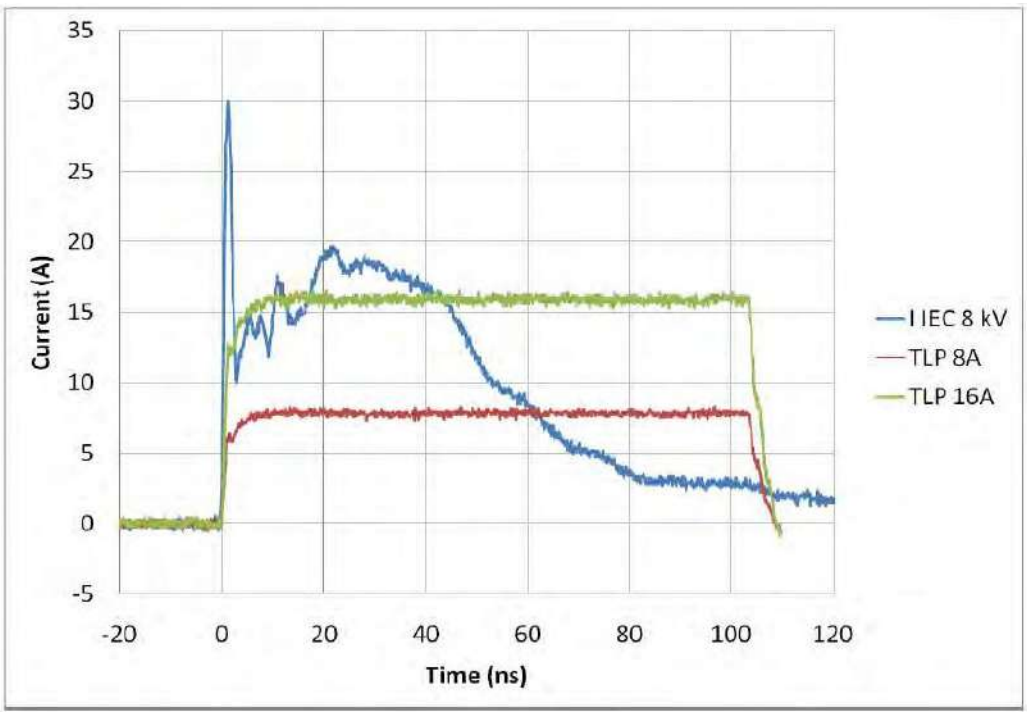
Figure 6. Typic Capacitance vs. Reverse Voltage



TYPIC CHARACTERISTICS

Figure 7. Transmission Line Pulse (TLP)

Transmission Line Pulse (TLP) is a measurement technique used in the Electrostatic Discharge (ESD) arena to characterize performance attributes of devices under ESD stresses. TLP is able to obtain current versus voltage (I−V) curves in which each data point is obtained with a 100 ns long pulse, with currents up to 40 A. TLP was first used in the ESD field to study human body model (HBM) in integrated circuits, but it is an equally valid tool in the field of system level ESD. The applicability of TLP to system level ESD is illustrated in Figure 1, which compares an 8 kV IEC 61000−4−2 current waveform with TLP current pulses of 8 and 16 A. The current levels and time duration for the pulses are similar and the initial rise time for the TLP pulse is comparable to the rise time of the IEC 61000−4−2's initial current spike. This application note will give a basic introduction to TLP measurements and explain the datasheet parameters extracted from TLP for SDI Technology's protection products.



Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

Comparison of a CurrentWaveform of IEC 61000−4−2with TLP Pulses at 8 and 16 A.
The IEC 61000−4−2 ESD waveforms is true to the Standard and is shown here as captured on an oscilloscope.
The points A, B, and C show the points on the aveforms specified in IEC 61000−4−2.
Transmission Line Pulse (TLP) Version.

APPLICATION INFORMATION

Figure 8. Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

1. Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.

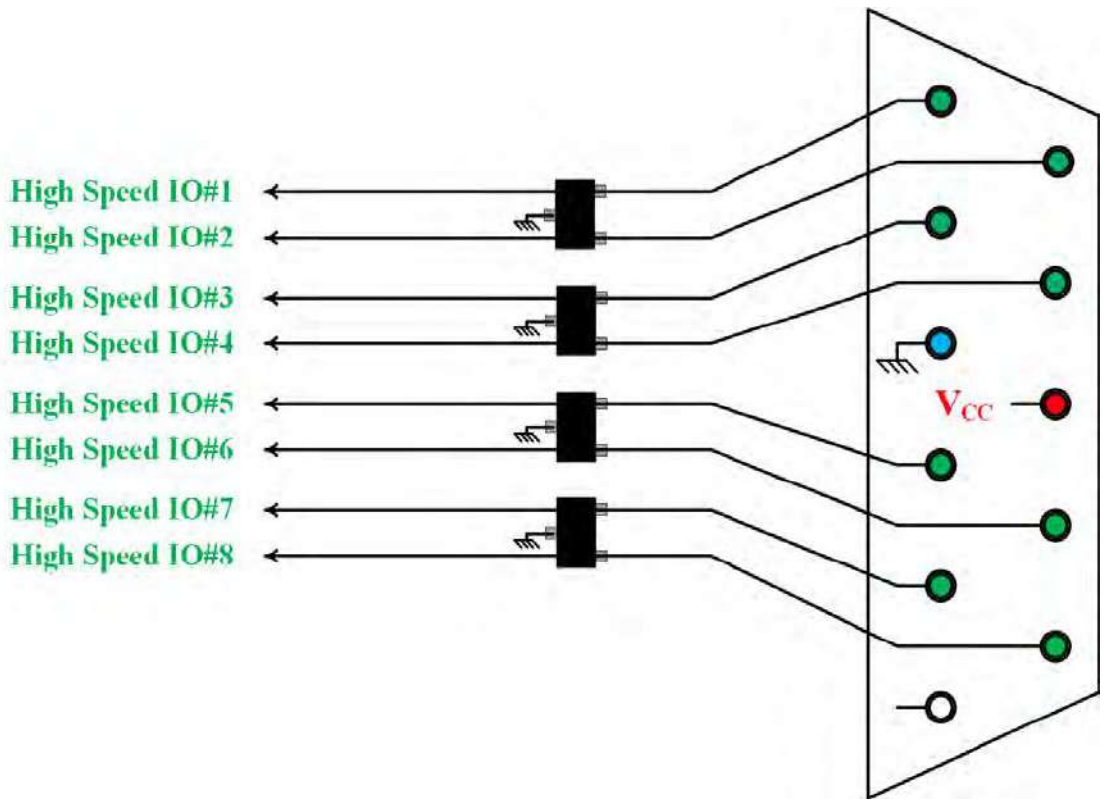
1.1. In USB 3.0/3.1 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in below drawing In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition. For more information on latchup considerations, see below description on below drawing.

2. Make sure to use differential design methodology and impedance matching of all high speed signal traces.

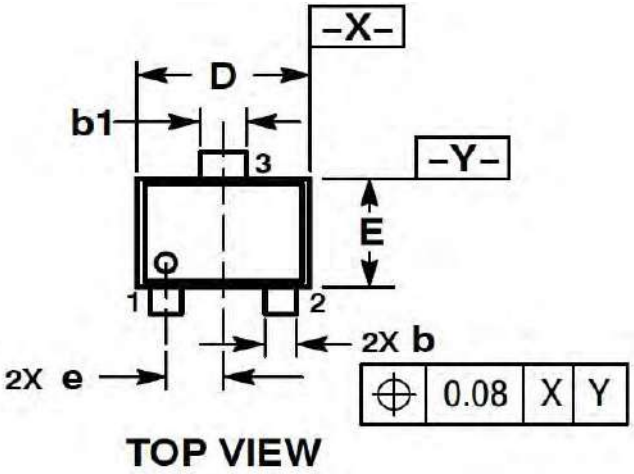
2.1. Use curved traces when possible to avoid unwanted reflections.

2.2. Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.

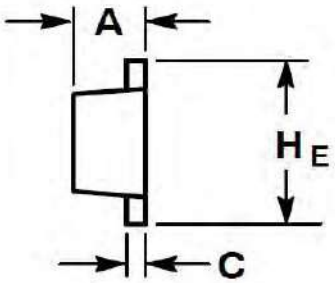
2.3. Place grounds between high speed pairs and keep asmuch distance between pairs as possible to reduce crosstalk.



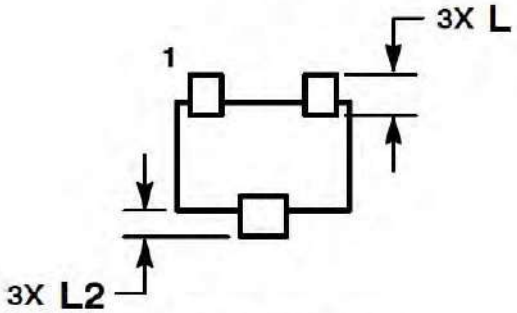
SOT-723 PACKAGE OUTLINE & DIMENSIONS



TOP VIEW



SIDE VIEW



BOTTOM VIEW

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
C	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H E	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25

* SOLDERING FOOTPRINT