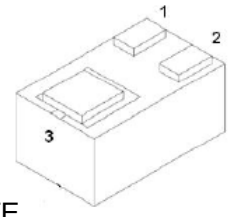
P-Channel Enhancement Mode Power MOSFET

Features:

- Lead Free Product is Acquired
- Surface Mount Package
- P-Channel Switch with Low R_{DS}(on)
- Operated at Low Logic Level Gate Drive
- ESD Protected Gate

DFN1006-3

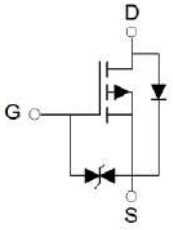


1.GATE
2.SOURCE
3.DRAIN

Applications:

- Load/ Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

Equivalent Circuit



MARKING:

P-Channel MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
-25V	560 mΩ@-4.5V	-0.6A
	780mΩ@-2.5V	
	950 mΩ(TYP)@-1.8V	

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-25	V
Typical Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current (note 1)	I_D	-0.6	A
Pulsed Drain Current (tp=10us)	I_{DM}	-1.2	A
Power Dissipation (note 2)	P_D	100	mW
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	1250	℃/W
Operation Junction and Storage Temperature Range	T_J,T_{STG}	-55~ 150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10 s)	T_L	260	℃

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25 ℃ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-25	-27		V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-20V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±10V, V_{DS} = 0V			±20	uA
Gate threshold voltage (note 2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.35		-1.1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-1A		430	560	mΩ
		V_{GS} =-2.5V, I_D =-0.8A		624	780	mΩ
		V_{GS} =-1.8V, I_D =-0.5A		950		mΩ
Forward tranconductance(note 2)	g_{FS}	V_{DS} =-10V, I_D =-0.54A		1.2		S
Diode forward voltage	V_{SD}	I_S=-0.5A, V_{GS} = 0V			-1.2	V
DYNAMIC PARAMETERS(note 4)						
Input Capacitance	C_{iss}	V_{DS} =-16V,V_{GS} =0V,f =1MHz		113	170	pF
Output Capacitance	C_{oss}			15	25	pF
Reverse Transfer Capacitance	C_{rss}			9	15	pF
SWITCHING PARAMETERS (note 4)						
Turn-on delay time (note 3)	$t_{d(on)}$	V_{DD}=-4.5V,V_{GS}=-10V, I_D=-200mA,R_{GEN}=10Ω		9		ns
Turn-on rise time (note 3)	t_r			5.8		ns
Turn-off delay time (note 3)	$t_{d(off)}$			32.7		ns
Turn-off fall time (note 3)	t_f			20.3		ns

Notes :

1.Surface mounted on FR4 board using the minimum recommended pad size.

2. Pulse Test : Pulse width=300μs, duty cycle≤2%.

3. Switching characteristics are independent of operating junction temperatures.

4. Graranted by design，not subject to producting.

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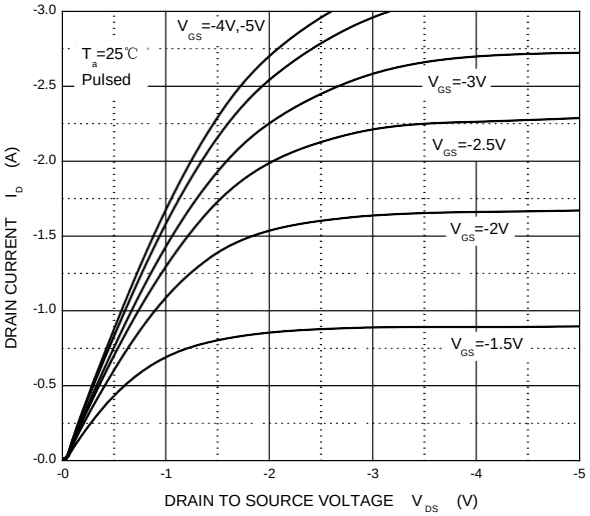
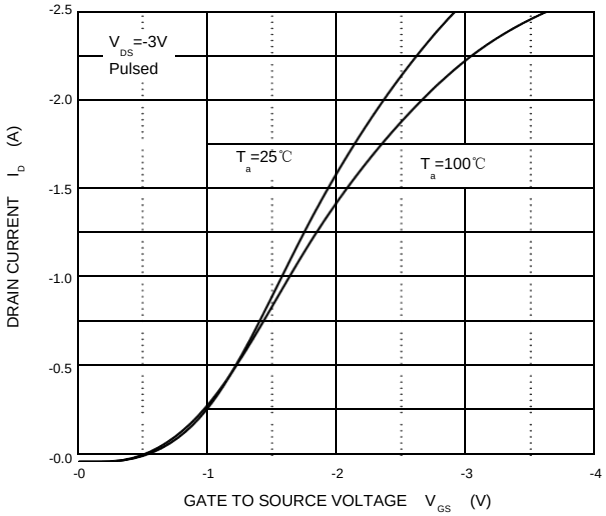
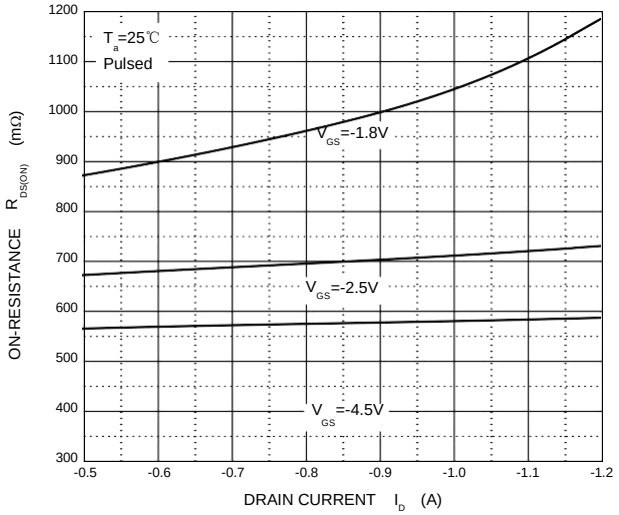
Output Characteristics



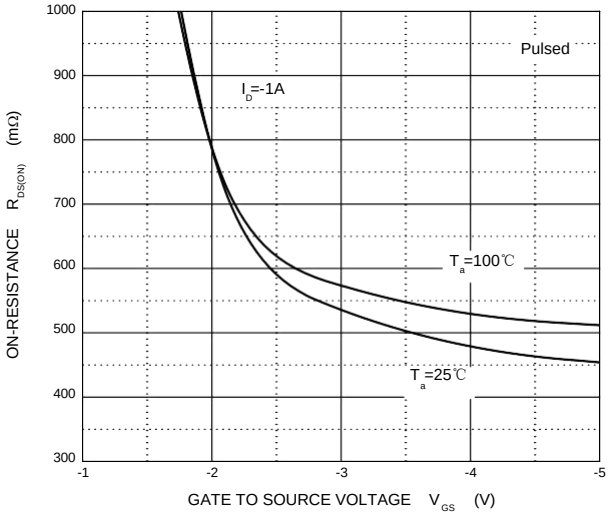
Transfer Characteristics



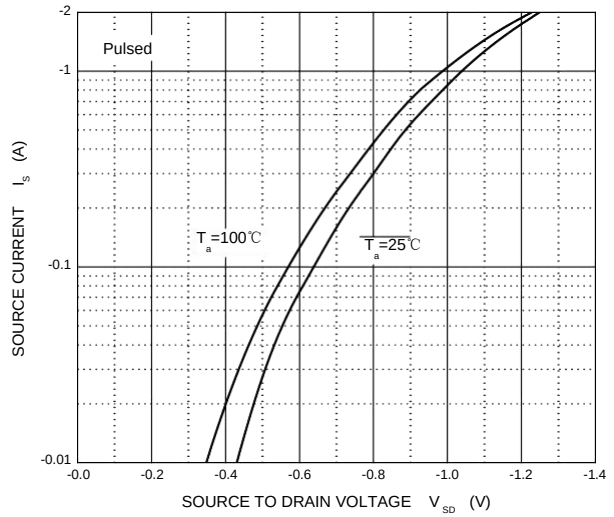
$R_{DS(ON)}$ — I_D



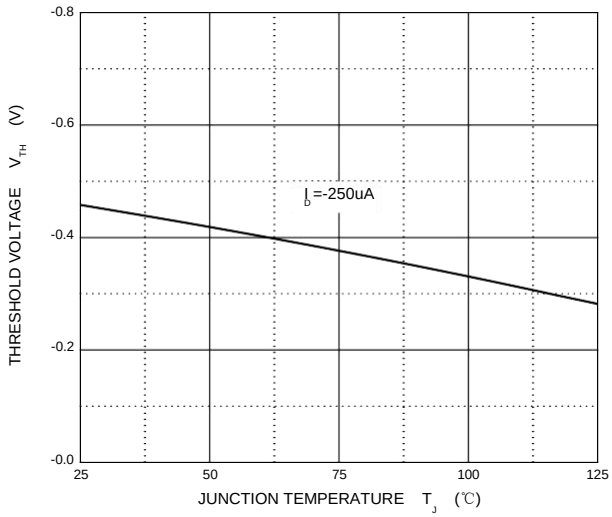
$R_{DS(ON)}$ — V_{GS}



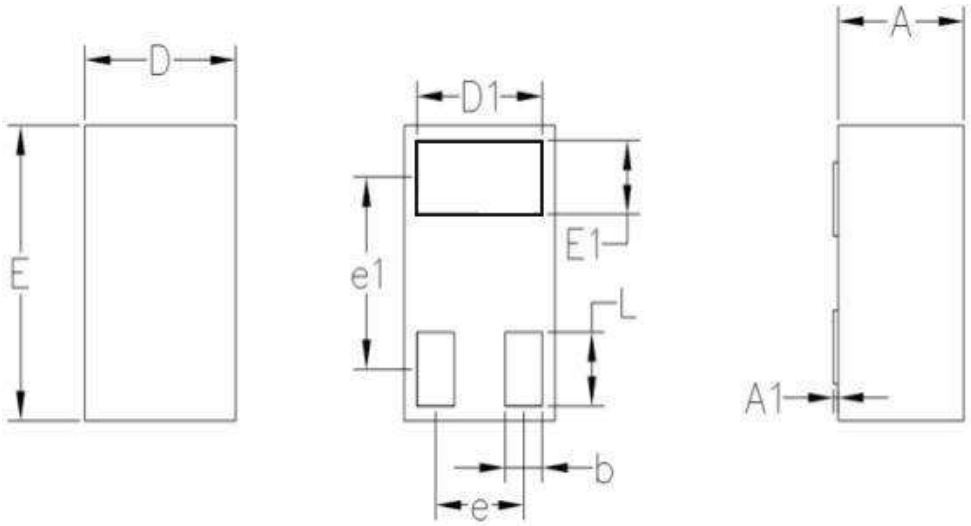
I_S — V_{SD}



Threshold Voltage



DFN1006-3 **Package Outline Dimensions**



SYMBOL	DIMENSIONS IN MM		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	—	0.05
D	0.55	0.60	0.65
E	0.95	1.00	1.05
D1	045	0.50	0.55
E1	0.20	0.25	0.30
L	0.20	0.25	0.30
b	0.10	0.15	0.20
e	0.35BSC		
e1	0.65BSC		