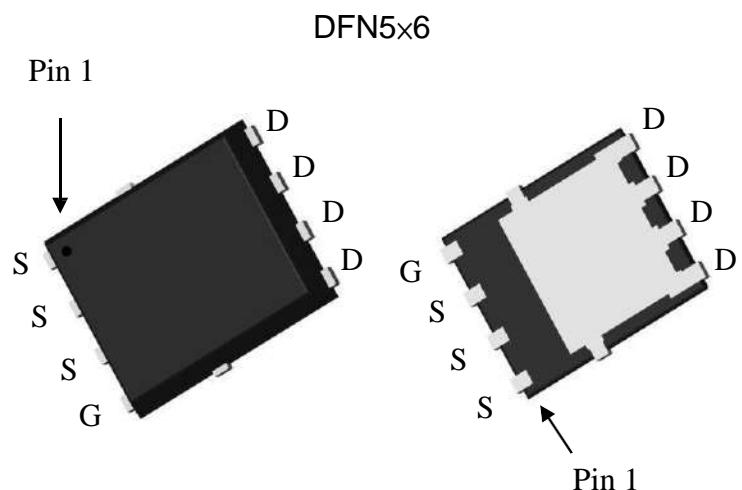


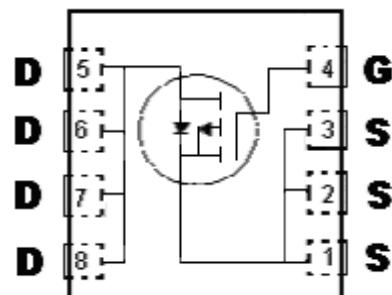
## P-Channel Enhancement Mode Power MOSFET

### Features:

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package



<b>BV<sub>DSS</sub></b>		-20V
ID@V <sub>GS</sub> =-4.5V, T <sub>C</sub> =25°C		-85.5A
ID@V <sub>GS</sub> =-4.5V, T <sub>A</sub> =25°C		-27A
R <sub>DSON(TYP)</sub>	V <sub>GS</sub> =-4.5V, ID=-20A	2.0mΩ
	V <sub>GS</sub> =-2.5V, ID=-20A	2.6mΩ



G : Gate D : Drain S : Source

### Ordering Information

Device	Package	Shipping
KWA2D0P02H8	DFN5x6 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel

## Absolute Maximum Ratings ( $T_a=25^{\circ}\text{C}$ )

Parameter	Symbol	10s	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-20		V
Gate-Source Voltage	$V_{GS}$	$\pm 8$		
Continuous Drain Current @ $T_c=25^{\circ}\text{C}$ , $V_{GS}=-4.5\text{V}$ (Note1)	$I_D$	-85.5 (silicon limit)		A
Continuous Drain Current @ $T_c=100^{\circ}\text{C}$ , $V_{GS}=-4.5\text{V}$ (Note1)		-54.0 (silicon limit)		
Continuous Drain Current @ $T_c=25^{\circ}\text{C}$ , $V_{GS}=-4.5\text{V}$ (Note1)		-43 (package limit)		
Continuous Drain Current @ $T_a=25^{\circ}\text{C}$ , $V_{GS}=-4.5\text{V}$ (Note2)	$I_{DSM}$	-27	-17.5	
Continuous Drain Current @ $T_a=70^{\circ}\text{C}$ , $V_{GS}=-4.5\text{V}$ (Note2)		-21.6	-14.0	
Pulsed Drain Current (Note3)	$I_{DM}$	-287		
Avalanche Current @ $L=0.1\text{mH}$	$I_{AS}$	-82		
Avalanche Energy @ $L=0.5\text{mH}$ , $I_D=-50\text{A}$ , $V_{DD}=-15\text{V}$ (Note4)	$E_{AS}$	625		mJ
Total Power Dissipation	$P_D$	50		W
		20		
	$P_{DSM}$	5.0	2.1	
		3.2	1.3	
Operating Junction and Storage Temperature Range	$T_j$ , $T_{stg}$	-55~+150		°C

## Thermal Data

Parameter	Symbol	Typical	Maximum	Unit
Thermal Resistance, Junction-to-case	$R_{th,j-c}$	2	2.5	
Thermal Resistance, Junction-to-ambient (Note2)	$R_{th,j-a}$	18	25	°C/W
		50	60	

- Note : 1. The power dissipation  $P_D$  is based on  $T_{j(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.  
 2. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with  $T_a=25^{\circ}\text{C}$ . The power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^{\circ}\text{C}$ . The value in any given application depends on the user's specific board design.  
 3. Pulse width limited by junction temperature  $T_{j(MAX)}=150^{\circ}\text{C}$ . Ratings are based on low frequency and low duty cycles to keep initial  $T_j=25^{\circ}\text{C}$ .  
 4. 100% tested by conditions of  $L=0.1\text{mH}$ ,  $V_{GS}=-10\text{V}$ ,  $I_{AS}=-40\text{A}$ ,  $V_{DD}=-15\text{V}$

## Characteristics ( $T_c=25^{\circ}\text{C}$ , unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
$BV_{DSS}$	-20	-	-		$V_{GS}=0\text{V}$ , $I_D=-250\mu\text{A}$
$V_{GS(th)}$	-0.5	-	-1.2	V	$V_{DS} = V_{GS}$ , $I_D=-250\mu\text{A}$
$G_{FS}$ *1	-	82.8	-	S	$V_{DS}=-10\text{V}$ , $I_D=-20\text{A}$
$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 8\text{V}$ , $V_{DS}=0\text{V}$
$I_{DSS}$	-	-	-1	$\mu\text{A}$	$V_{DS}=-16\text{V}$ , $V_{GS}=0\text{V}$
	-	-	-25		$V_{DS}=-16\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=125^{\circ}\text{C}$

$R_{DS(on)} *1$	-	2.0	2.8	$m\Omega$	$V_{GS} = -4.5V, I_D = -20A$
	-	2.6	4.5		$V_{GS} = -2.5V, I_D = -20A$
<b>Dynamic *4</b>					
$C_{iss}$	-	19369	-	pF	$V_{DS} = -20V, V_{GS} = 0V, f = 1MHz$
$C_{oss}$	-	1442	-		
$C_{rss}$	-	550	-		
$Q_g *1, 2$	-	218	-		
$Q_{gs} *1, 2$	-	30	-		
$Q_{gd} *1, 2$	-	81	-		
$t_{d(ON)} *1, 2$	-	30.8	-		
$t_r *1, 2$	-	29	-		
$t_{d(OFF)} *1, 2$	-	294	-		
$t_f *1, 2$	-	114	-		
$R_g$	-	1.8	-	$\Omega$	$f = 1MHz$
<b>Source-Drain Diode</b>					
$V_{SD} *1$	-	-0.8	-1.2	$V$	$I_S = -20A, V_{GS} = 0V$
$t_{rr}$	-	42	-	ns	$I_F = -20A, dI_F/dt = 100A/\mu s$
$Q_{rr}$	-	47	-	nC	

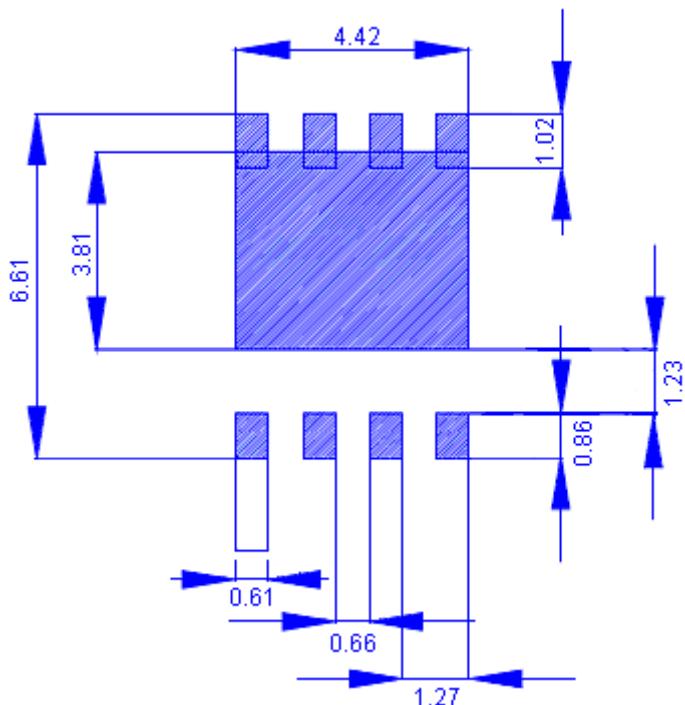
Note : \*1.Pulse Test : Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$

\*2.Independent of operating temperature

\*3.Pulse width limited by maximum junction temperature.

\*4.Guaranteed by design, not subject to production testing.

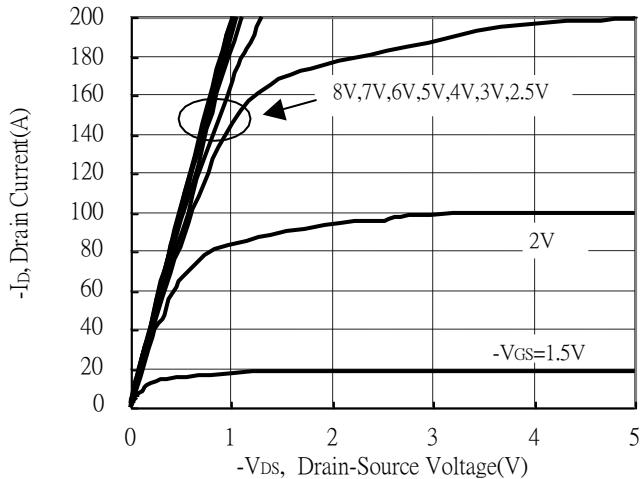
## Recommended Soldering Footprint



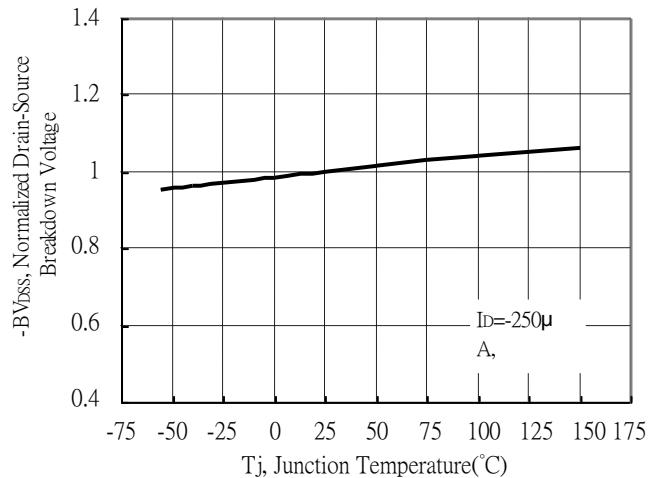
unit : mm

## Typical Characteristics

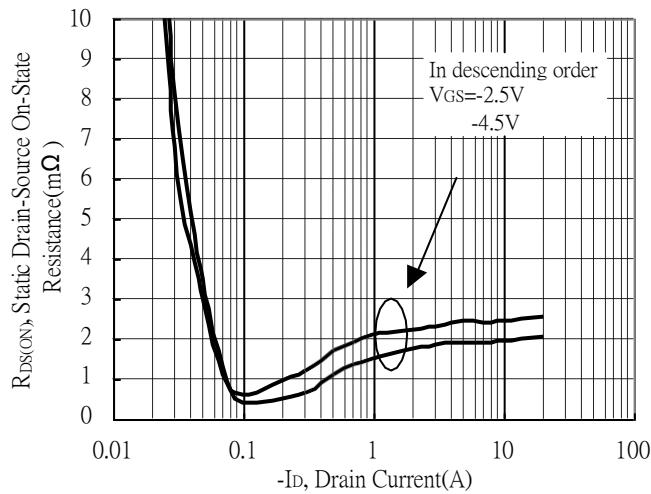
Typical Output Characteristics



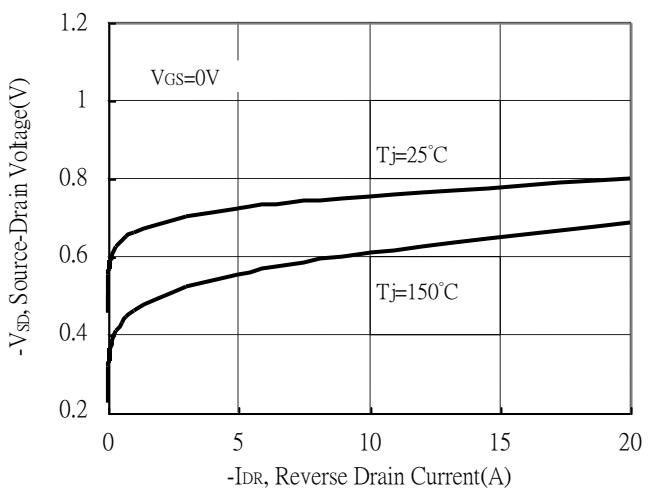
Breakdown Voltage vs Ambient Temperature



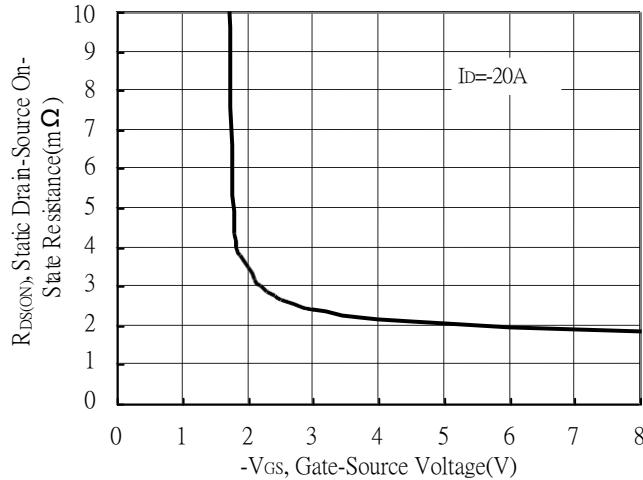
Static Drain-Source On-State resistance vs Drain Current



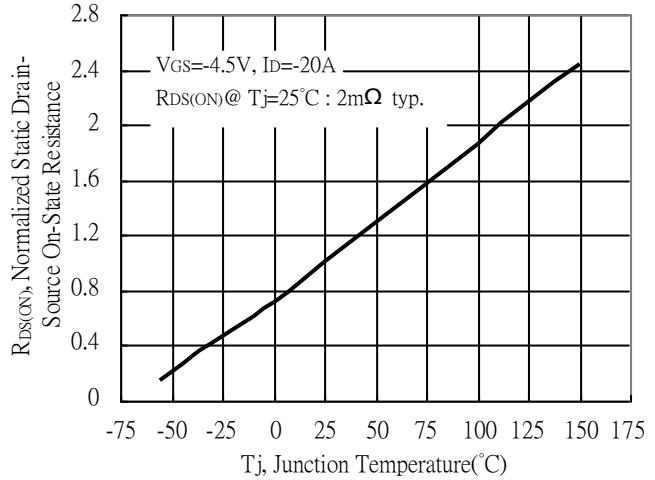
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

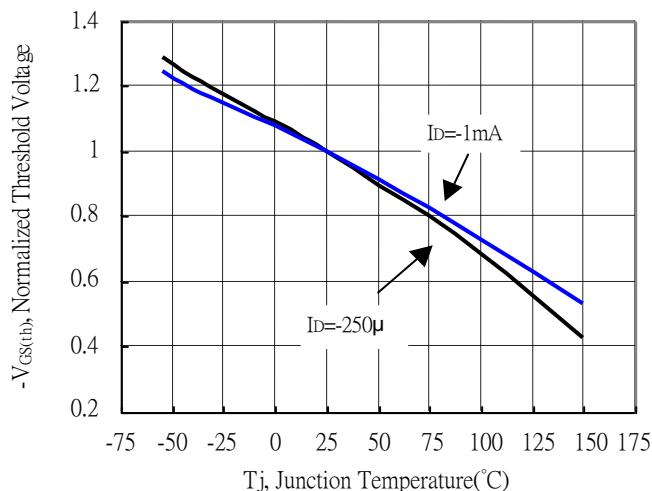


Drain-Source On-State Resistance vs Junction Temperature

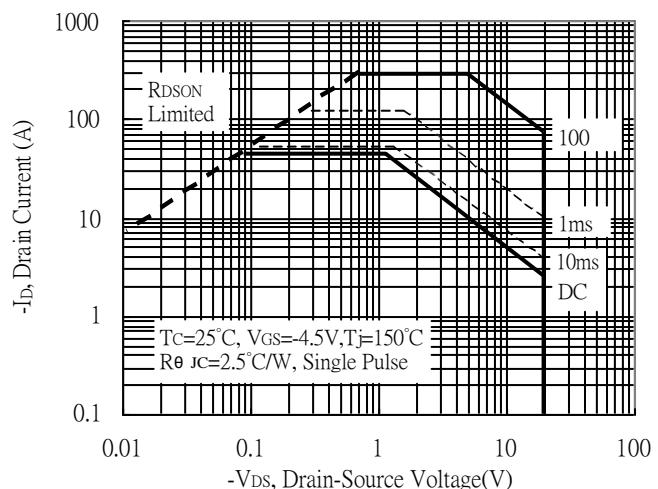


## Typical Characteristics(Cont.)

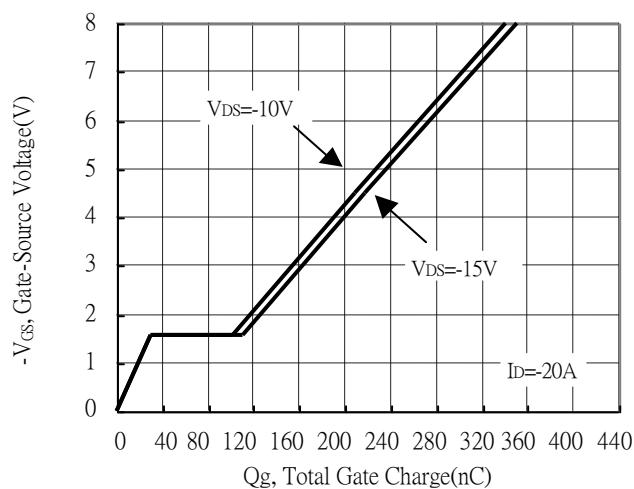
Threshold Voltage vs Junction Temperature



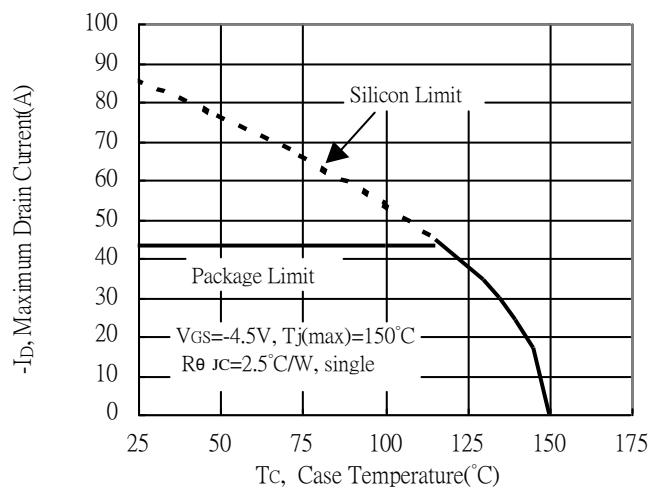
Maximum Safe Operating Area



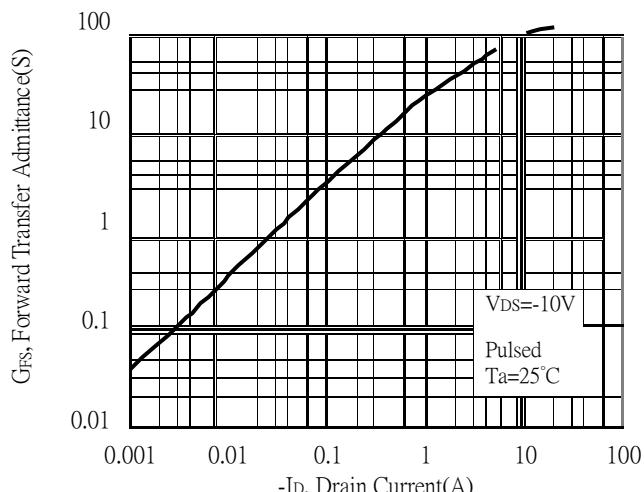
Gate Charge Characteristics



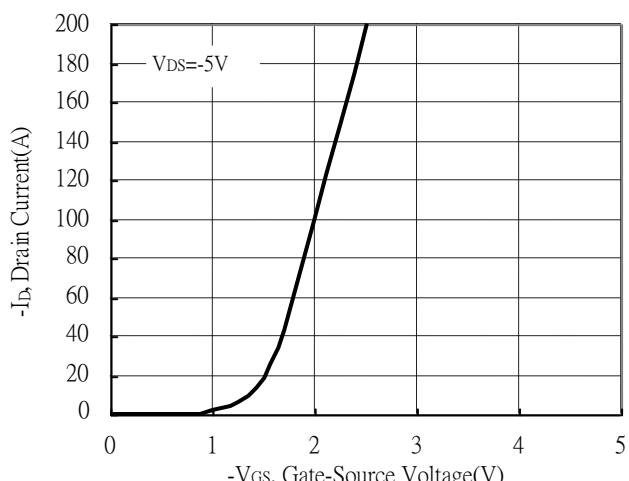
Maximum Drain Current vs Case Temperature



Forward Transfer Admittance vs Drain Current

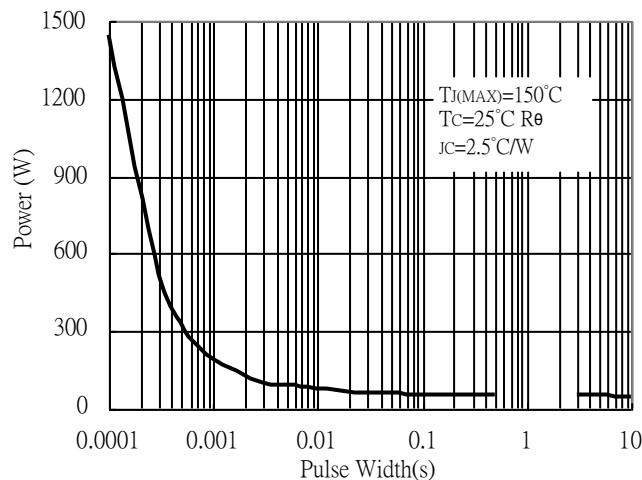


Typical Transfer Characteristics

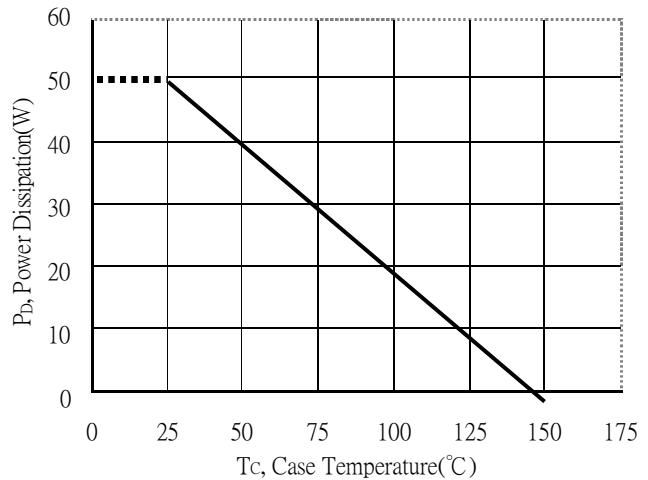


## Typical Characteristics(Cont.)

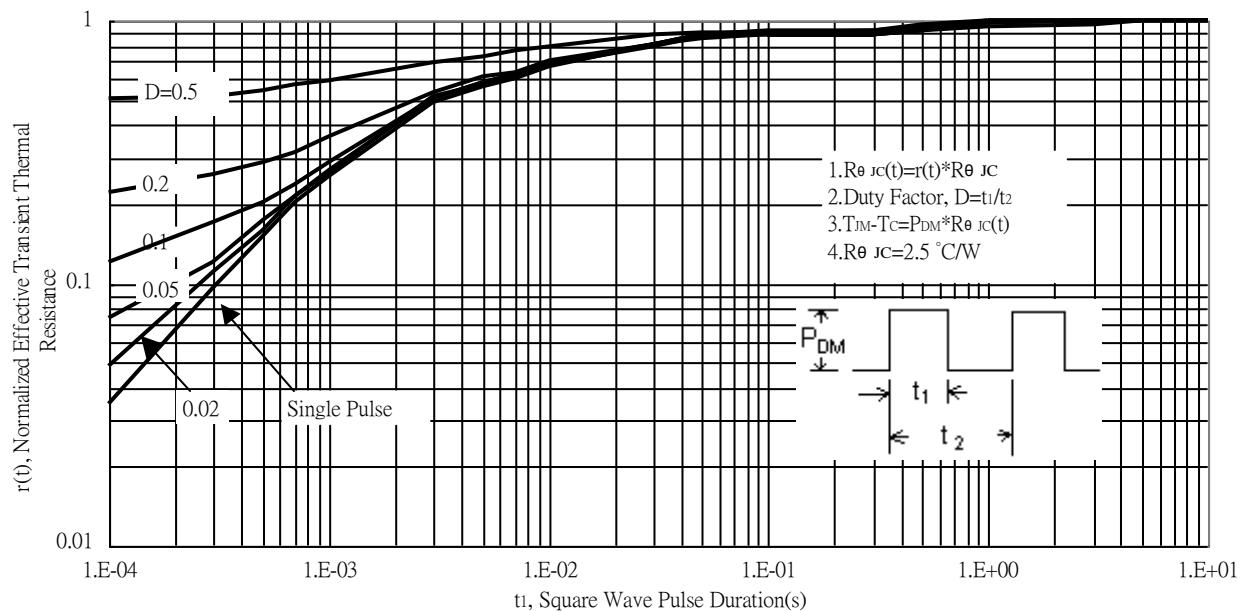
Single Pulse Maximum Power Dissipation



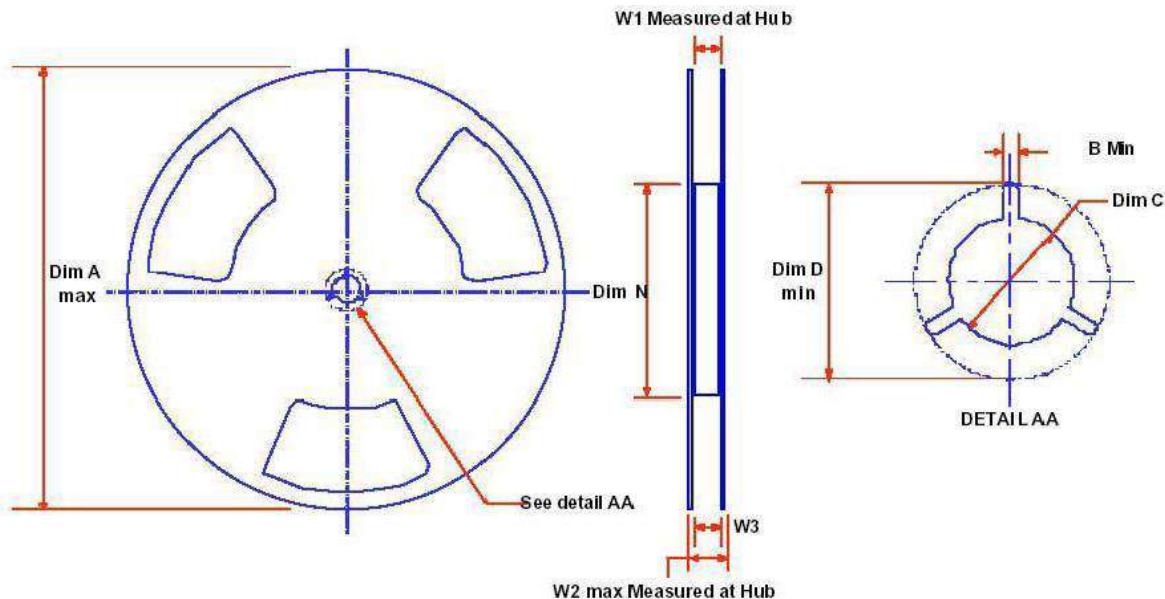
Power Derating Curve



Transient Thermal Response Curves



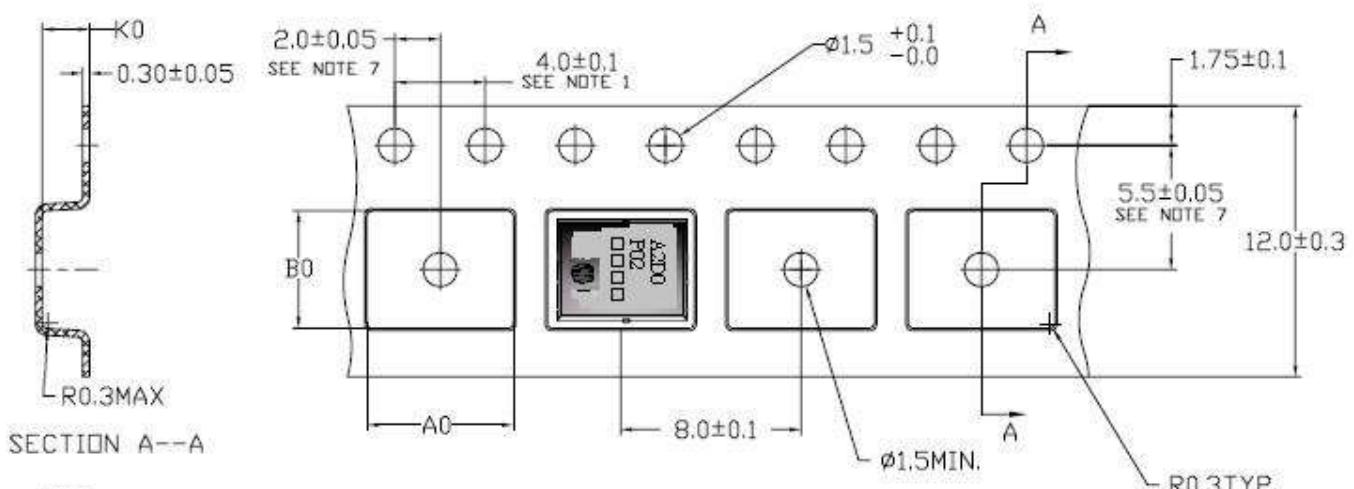
## Reel Dimension



Dimensions are in inches and millimeters

Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm.	13" Dia (STD/L99Z)	13.00 330 $\pm$ 1	0.069 1.5 Min.	0.512 13.0 Min.	0.795 20.2(ref.)	7.00 178 $\pm$ 2	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4(ref.)	0.469 - 0.606 11.9 - 15.4

## Carrier Tape Dimension



NOTE:

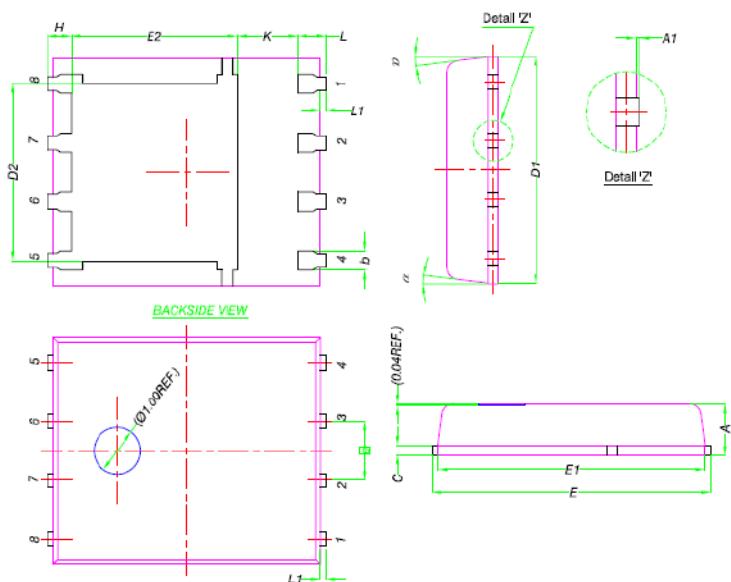
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE  $\pm$ 0.2
2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm.
3. MATERIAL BLACK STATIC DISSIPATIVE PS.(POLYSTYRENE)
4. ALL DIMENSIONS ARE IN MILLIMETERS (UNLESS OTHERWISE SPECIFIED)
5. A0 AND B0 MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
6. K0 MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
7. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
- B. SURFACE RESISTIVITY  
 $1 \times 10^4$ ~ $1 \times 10^{11}$  OHMS/SQ  
 $1 \times 10^4$ ~ $1 \times 10^6$  OHMS/SQ. For Fairchild Only

$$A0 = 6.5 \pm 0.1$$

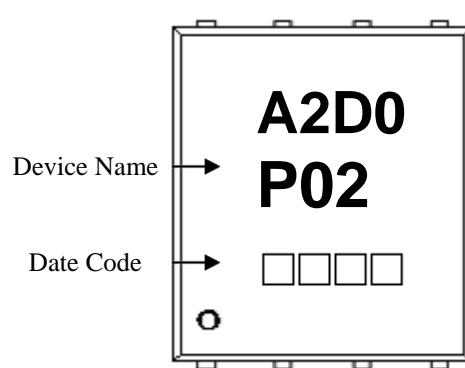
$$B0 = 5.3 \pm 0.1$$

$$K0 = 1.4 \pm 0.1$$

## DFN5×6 Dimension



Marking:



8-Lead DFN5×6 Plastic Package  
 Package Code : H8

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	E2	3.38	3.78	0.133	0.149
A1	0.00	0.05	0.000	0.002	e	1.27	BSC	0.050	BSC
b	0.33	0.51	0.013	0.020	H	0.41	0.61	0.016	0.024
C	0.20	0.30	0.008	0.012	K	1.10	-	0.043	-
D1	4.80	5.00	0.189	0.197	L	0.51	0.71	0.020	0.028
D2	3.61	3.96	0.142	0.156	L1	0.06	0.20	0.002	0.008
E	5.90	6.10	0.232	0.240	θ	8°	12°	8°	12°
E1	5.70	5.80	0.224	0.228					