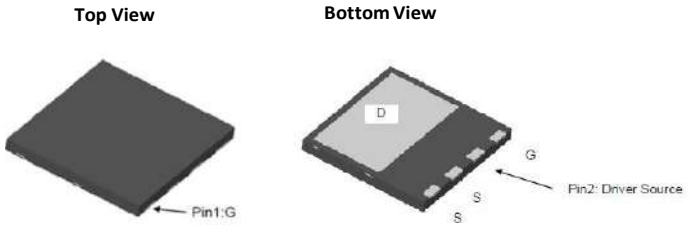
# 650V Super Junction Power MOSFET

## Features:

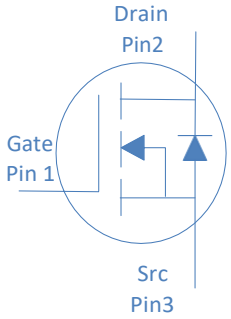
◇ High Speed Power Switching
◇ 100% UIS Tested, 100% Rg Tested
◇ Enhanced Avalanche Ruggedness
◇ Lead Free, Halogen Free

DFN8*8




## Application：

◇ SMPS
◇ Hard Switching and High Speed Circuit
◇ LED Lighting
◇ Flyback




| | | |
|---|---|---|
| $V_{DS}$ | 650 | V |
| $R_{DS(on),max}$ | 235 | mΩ |
| $I_D$ | 17 | A |

| Part Number | Package | Marking |
|---|---|---|
| KWSC65R235Y | DFN8*8 | SC65R235Y |

### Absolute Maximum Ratings at $T_j$=25℃ (unless otherwise specified)

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous Drain Current | $I_D$ | $T_C$=25℃ | 17 | A |
| Drain to Source Voltage | $V_{DS}$ | - | 650 | V |
| Gate to Source Voltage | $V_{GS}$ | - | ±30 | V |
| Pulsed Drain Current | $I_{DM}$ | - | 64 | A |
| Avalanche Energy, Single Pulse | $E_{AS}$ | $T_C$=25℃ | 505 | mJ |
| Power Dissipation | $P_D$ | $T_C$=25℃ | 278 | W |
| Operating and Storage Temperature | $T_J$, $T_{stg}$ | - | -55 to150 | ℃ |

### Absolute Maximum Ratings

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance Junction-Case | $R_{thJC}$ | 0.45 | ℃/W |
| Thermal Resistance Junction-Ambient | $R_{thJA}$ | 50 | ℃/W |

## Electrical Characteristics at $T_j$=25℃ (unless otherwise specified)

### Static Characteristics

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Drain to Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V, $I_D$=250μA | 650 | - | - | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$=$V_{DS}$, $I_D$=250μA | 2.4 | 3.4 | 4.4 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$=0V, $V_{DS}$=650V, $T_j$=25℃ | - | - | 1 | μA |
| Gate to Source Leakage Current | $I_{GSSF}$ | $V_{GS}$=30V, $V_{DS}$=0V | - | - | 100 | nA |
| | $I_{GSSR}$ | $V_{GS}$=-30V, $V_{DS}$=0V | - | - | -1 | μA |
| Drain to Source on Resistance | $R_{DS(on)}$ | $V_{GS}$=10V, $I_D$=8A | - | 196 | 235.2 | mΩ |
| Gate Resistance | $R_G$ | $V_{GS}$=0V, $V_{DS}$ Open, f=1MHz | - | 1.7 | - | Ω |

### Dynamic Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{iss}$ | $V_{GS}$=0V, $V_{DS}$=50V, f=1MHz | - | 1630 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 110 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 22.0 | - | |
| Effective output capacitance, energy related | $C_{O(er)}$ | VGS=0V, VDS=0…480V | - | 71 | - | |
| Effective output capacitance, time related | $C_{O(tr)}$ | | - | 301 | - | |
| Total Gate Charge | $Q_g$ | $V_{DD}$=480V, $I_D$=10A, $V_{GS}$=10V | - | 38.0 | - | nC |
| Gate to Source Charge | $Q_{gs}$ | | - | 10.6 | - | |
| Gate to Drain (Miller) Charge | $Q_{gd}$ | | - | 12.2 | - | |
| Turn on Delay Time | $t_{d(on)}$ | $V_{DD}$=400V, $I_D$=10A, $V_{GS}$=10V, $R_G$=3.4Ω, | - | 11 | - | ns |
| Rise time | $t_r$ | | - | 10 | - | |
| Turn off Delay Time | $t_{d(off)}$ | | - | 76 | - | |
| Fall Time | $t_f$ | | - | 8 | - | |

### Reverse Diode Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$ | $V_{GS}$=0V, $I_F$=10A | - | 0.83 | 1.1 | V |
| Reverse Recovery Time | $t_{rr}$ | $V_R$=400V, $I_F$=10A, $dI_F/dt$=100A/μs | - | 330 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 4.5 | - | μC |
| Reverse Recovery Charge | $I_{rm}$ | | - | 27.0 | - | μC |

Fig 1. Typical Output Characteristics

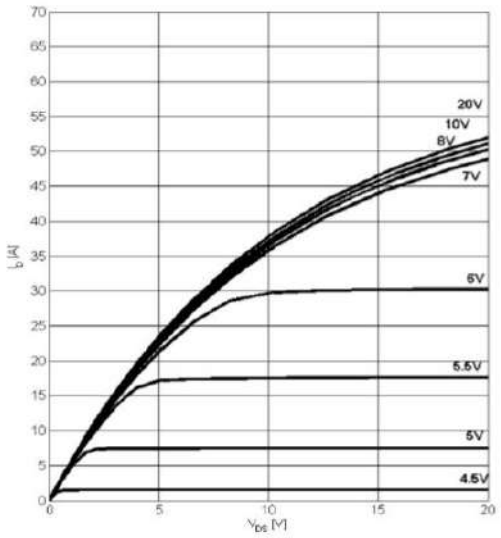



Figure 2. Typical Output Characteristics 125℃

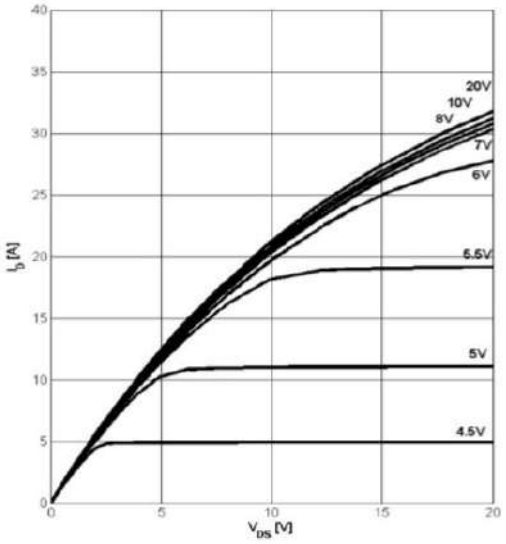



Figure 3. On-Resistance vs. Drain Current and Gate Voltage

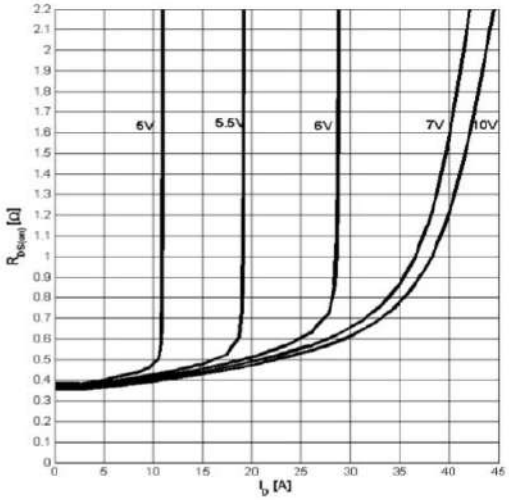



Figure 4. On-Resistance Variation vs. Junction Temperature

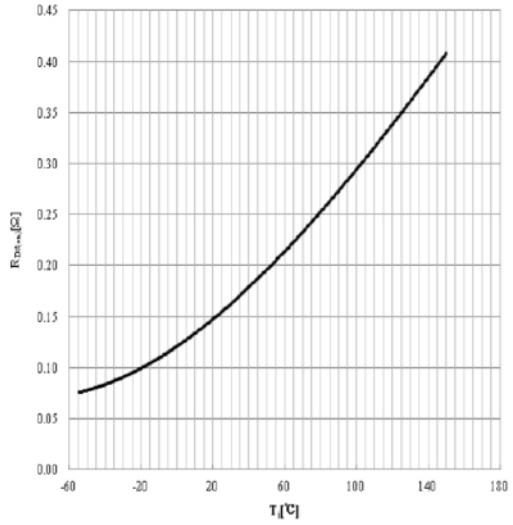



Figure 5. Typical Transfer Characteristics

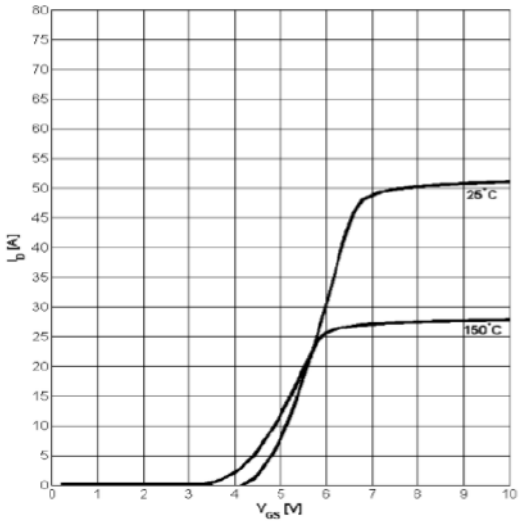



Figure 6:Typical Source-Drain Diode Forward Voltage

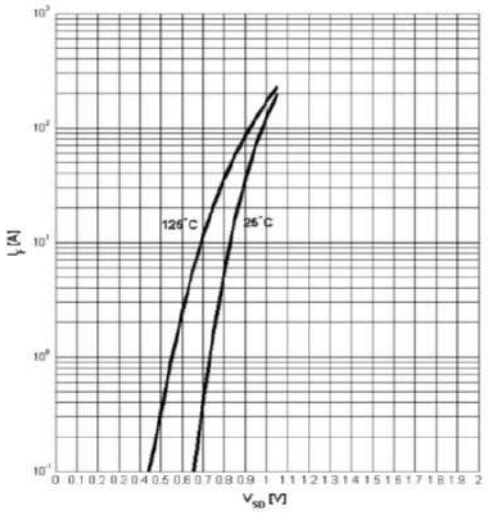


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

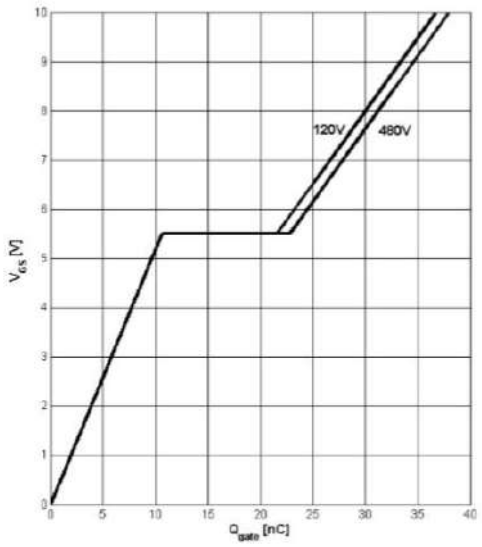



Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

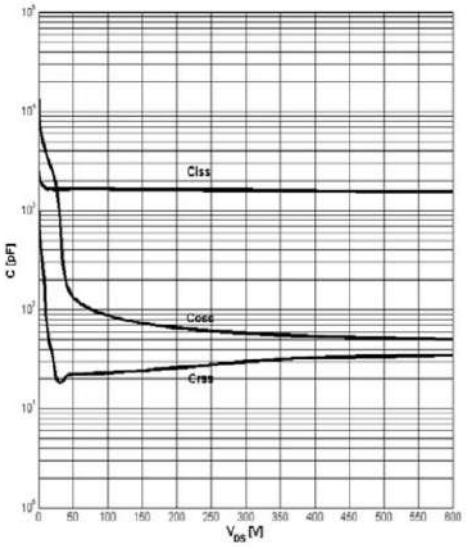



Figure 9. Maximum Safe Operating Area

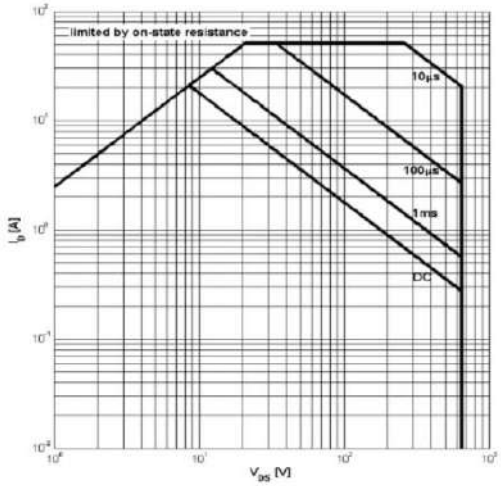



Figure 10. Power Dissipation

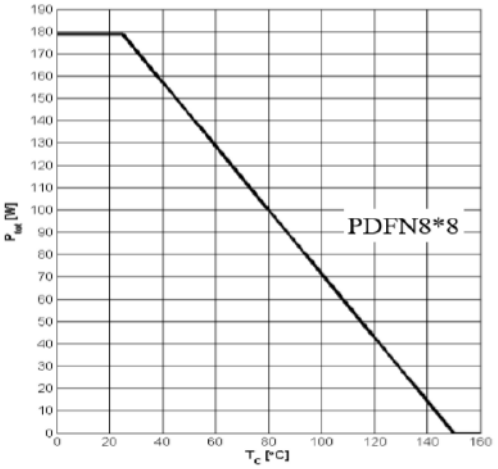



Figure 11. Normalized BV vs temperature

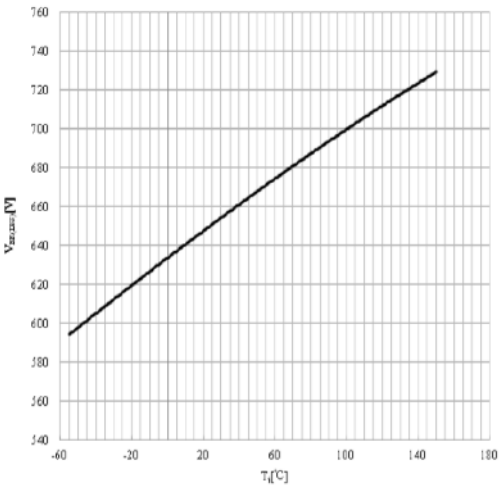
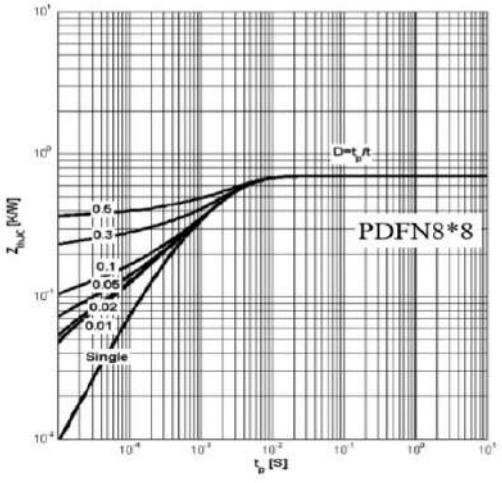
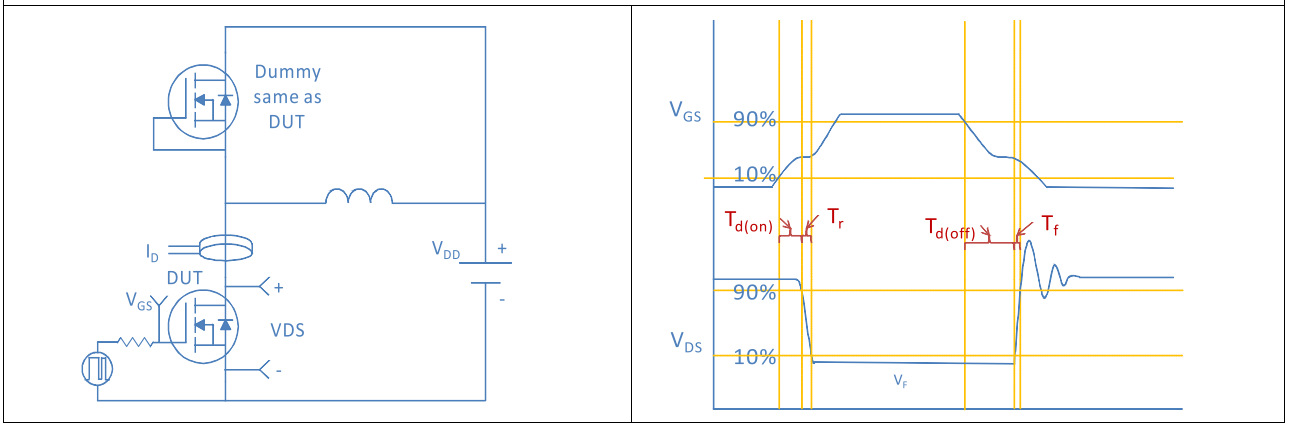


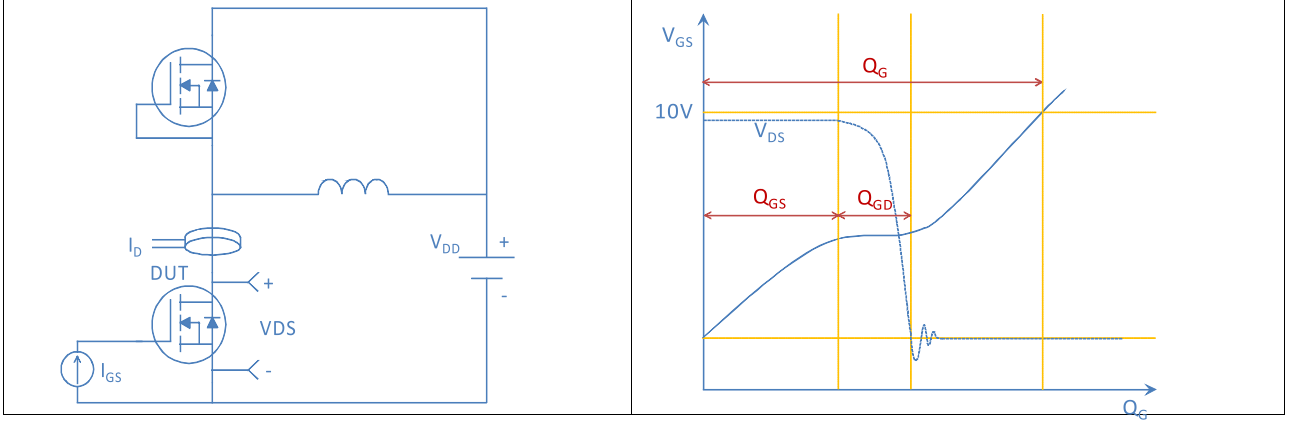

Figure 12. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



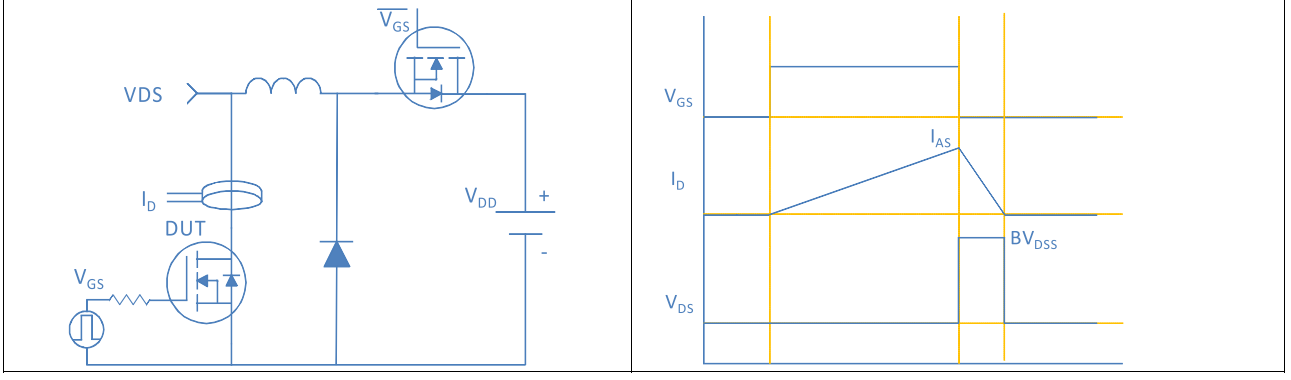
## Inductive switching Test



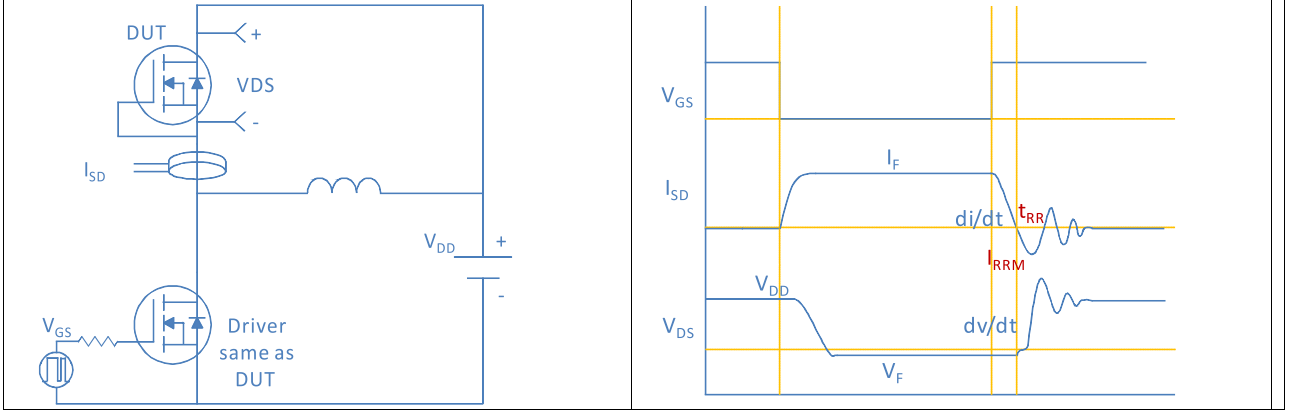

## Gate Charge Test




## Uclamped Inductive Switching (UIS) Test

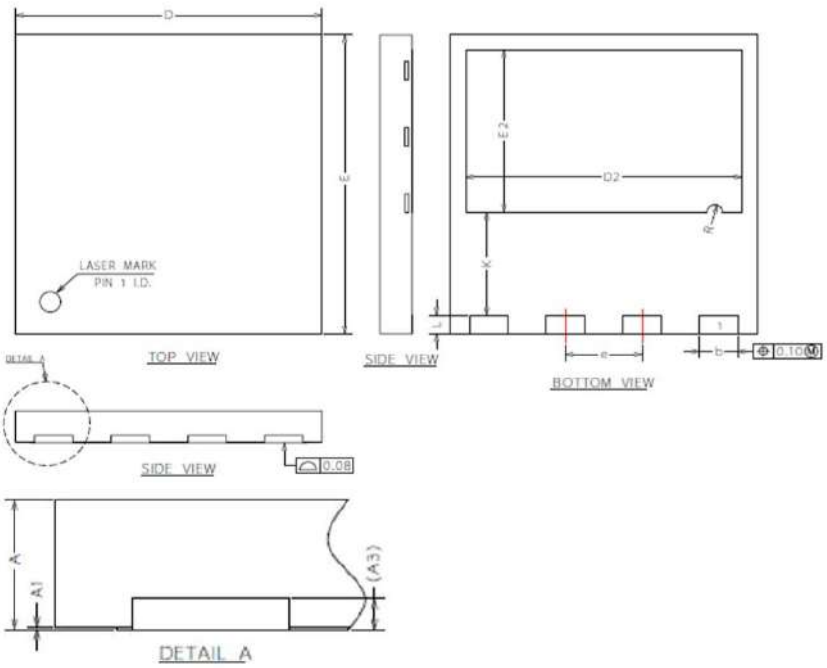



## Diode Recovery Test



Package Outline

DFN8*8




| Symbol | Dimensions(mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20REF | |
| b | 0.90 | 1.00 | 1.10 |
| D | 7.90 | 8.00 | 8.10 |
| D2 | 7.10 | 7.20 | 7.30 |
| E | 7.90 | 8.00 | 8.10 |
| E2 | 4.25 | 4.35 | 4.45 |
| e | | 2.00(BSC) | |
| K | 2.65 | 2.75 | 2.85 |
| L | 0.40 | 0.50 | 0.60 |
| R | | 0.20REF | |