

100V N-Ch Power MOSFET

Feature

- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free

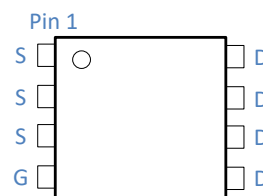
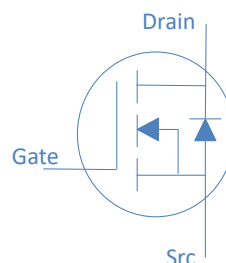
Application

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control

Part Number	Package	Marking
KPRGN035N10AL	DFN5x6	GN035N10AL

V_{DS}	100	V
$R_{DS(on),typ}$	$V_{GS}=10V$	3.1 $m\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	4.0 $m\Omega$
I_D (Silicon Limited)	149	A
I_D (Package Limited)	60	A

DFN5x6



Absolute Maximum Ratings at $T_J=25^{\circ}C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25^{\circ}C$	149	A
		$T_C=100^{\circ}C$	94	
Continuous Drain Current (Package Limited)		$T_C=25^{\circ}C$	60	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	530	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.1mH, T_C=25^{\circ}C$	180	mJ
Power Dissipation	P_D	$T_C=25^{\circ}C$	144	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	$^{\circ}C$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	0.87	$^{\circ}C/W$
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	55	$^{\circ}C/W$

Electrical Characteristics at $T_J=25^{\circ}\text{C}$ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.4	1.7	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=100V, T_J=25^{\circ}\text{C}$	-	-	1	μA
		$V_{GS}=0V, V_{DS}=100V, T_J=100^{\circ}\text{C}$	-	-	100	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	3.1	3.7	m Ω
		$V_{GS}=4.5V, I_D=10A$	-	4	5.2	
Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$	-	80	-	S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$	-	0.6	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=50V, f=1\text{MHz}$	-	5074	-	pF
Output Capacitance	C_{oss}		-	939	-	
Reverse Transfer Capacitance	C_{rss}		-	15.66	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=50V, I_D=20A, V_{GS}=10V$	-	90	-	nC
Gate to Source Charge	$Q_{gs}(4.5V)$		-	48	-	
Gate to Source Charge	Q_{gs}		-	12	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	26	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=20A, V_{GS}=10V, R_G=10\Omega,$	-	20	-	ns
Rise time	t_r		-	15	-	
Turn off Delay Time	$t_{d(off)}$		-	42	-	
Fall Time	t_f		-	10	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$V_R=50V, I_F=20A, dI_F/dt=100A/\mu s$	-	65	-	ns
Reverse Recovery Charge	Q_{rr}		-	104	-	nC

Fig 1. Typical Output Characteristics

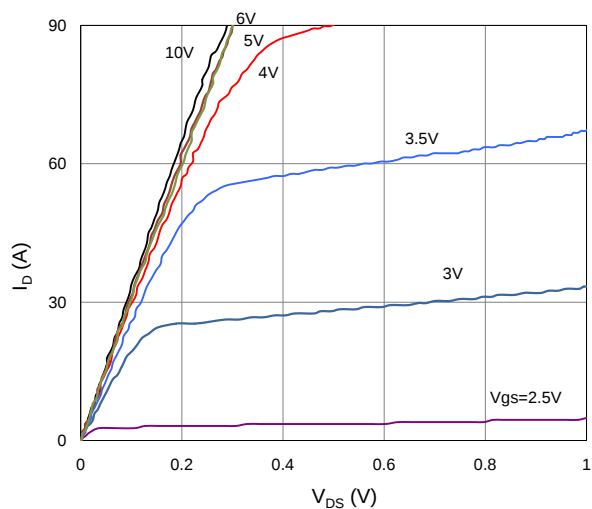


Figure 2. On-Resistance vs. Gate-Source Voltage

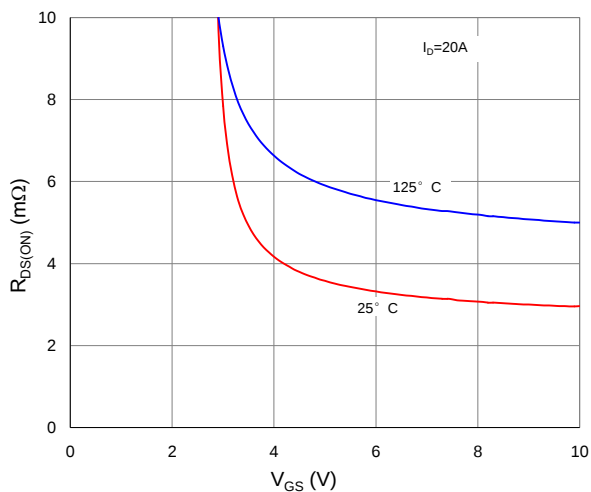


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

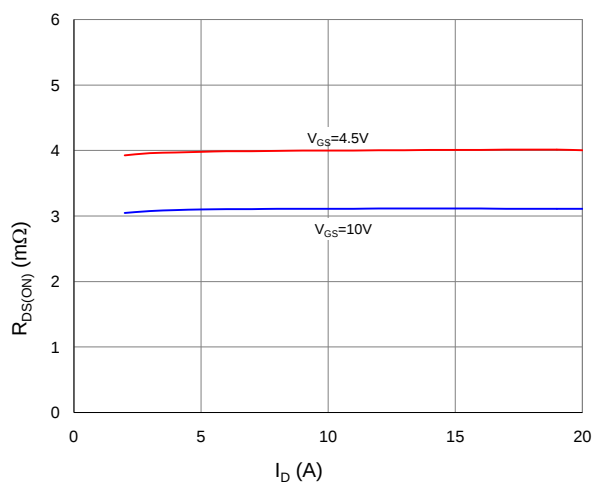


Figure 4. Normalized On-Resistance vs. Junction Temperature

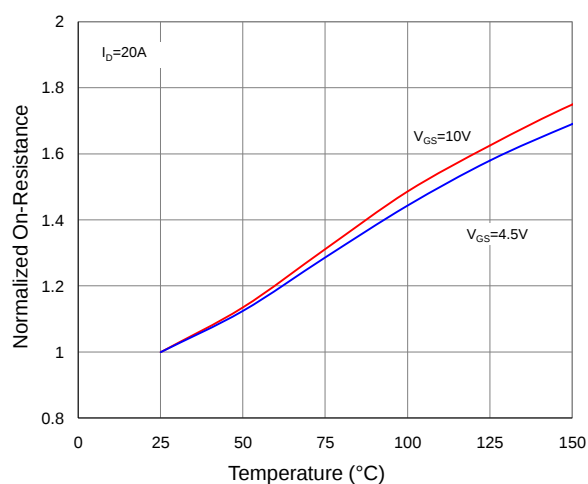


Figure 5. Typical Transfer Characteristics

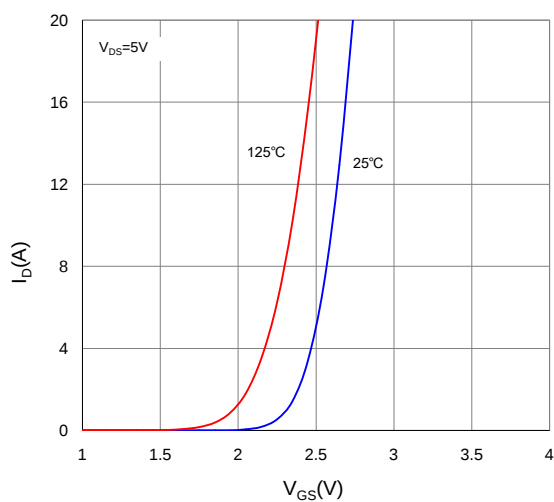


Figure 6. Typical Source-Drain Diode Forward Voltage

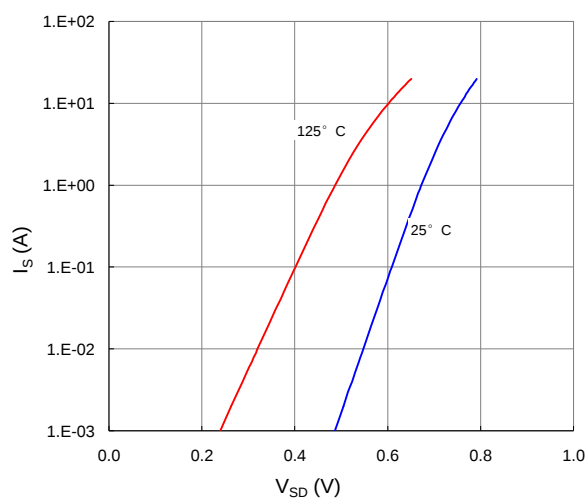


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

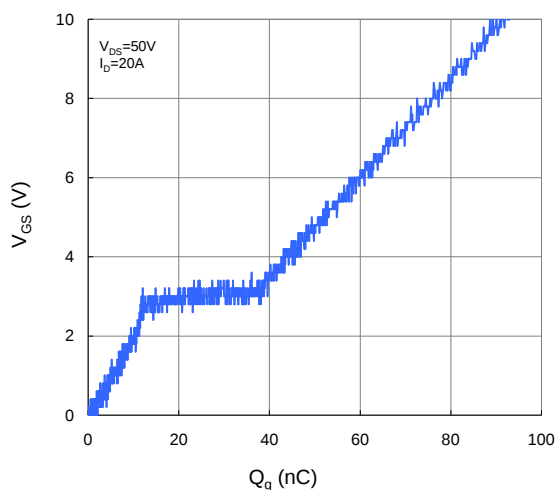


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

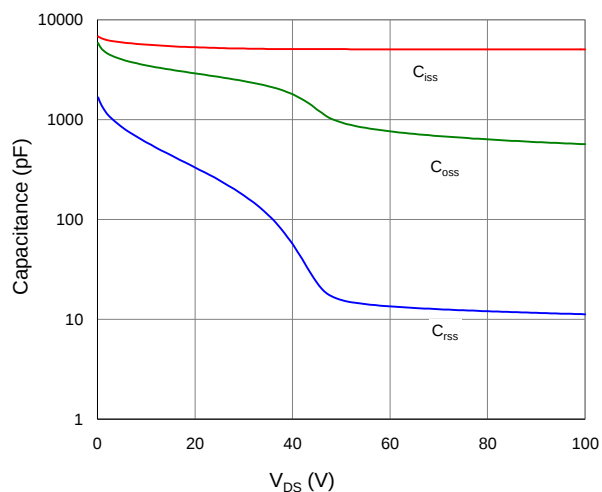


Figure 9. Maximum Safe Operating Area

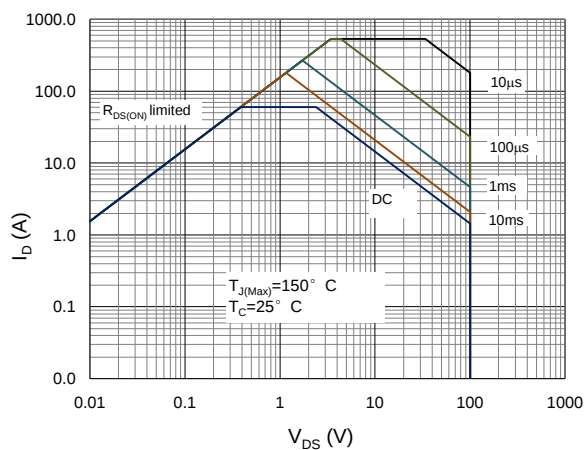


Figure 10. Maximum Drain Current vs. Case Temperature

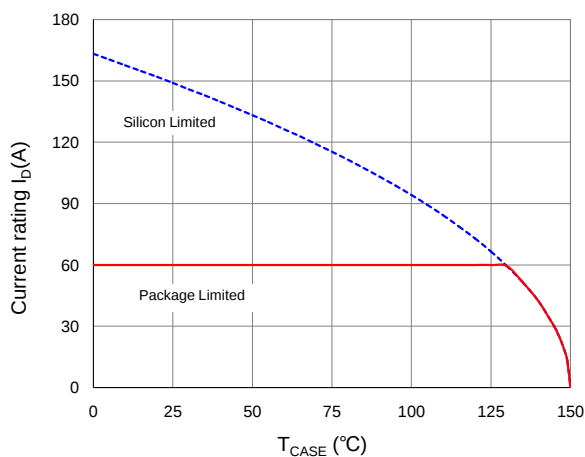
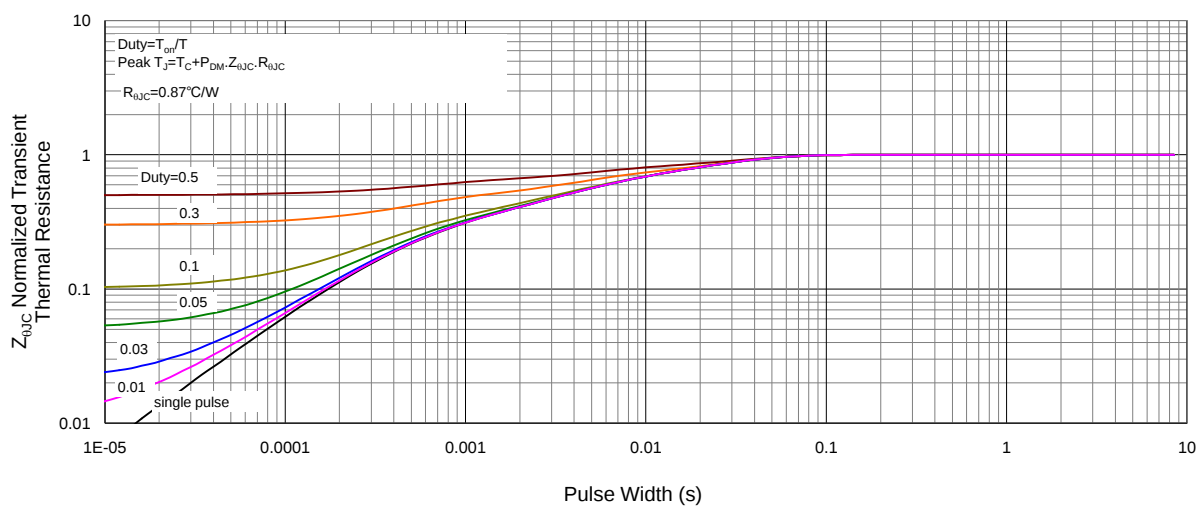
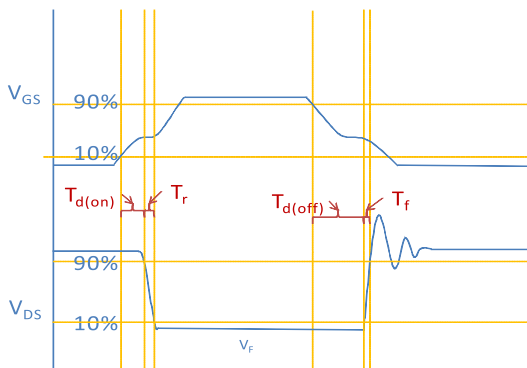
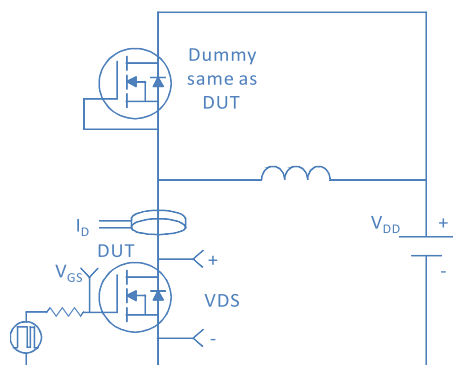


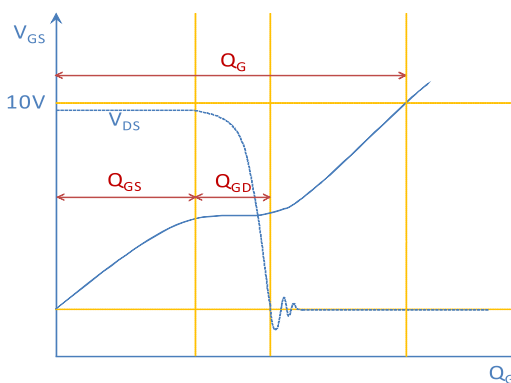
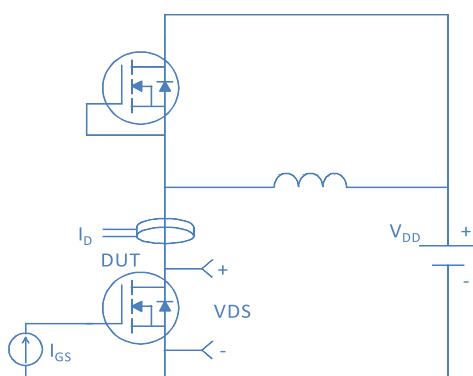
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



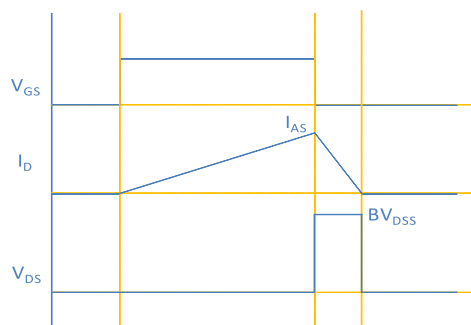
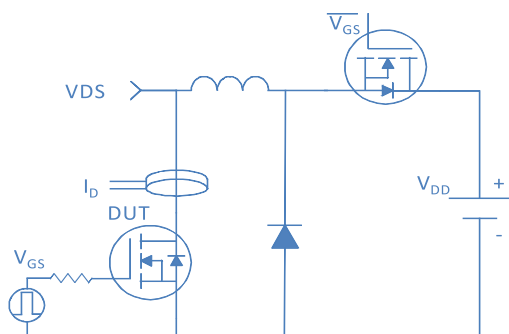
Inductive switching Test



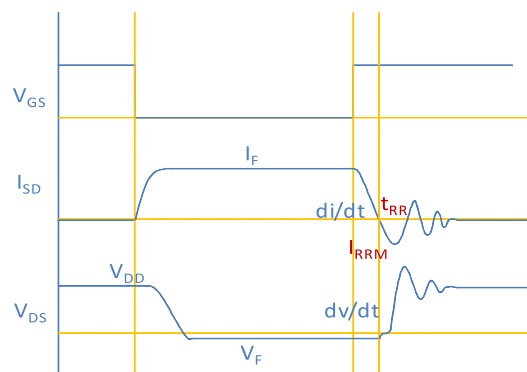
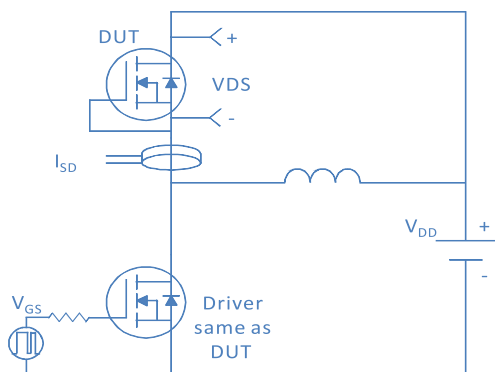
Gate Charge Test



Uclamped Inductive Switching (UIS) Test



Diode Recovery Test



DFN5x6_P, 8 Leads

