

80V N-Ch Power MOSFET

Features:

- ◇ High Speed Power Switching
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

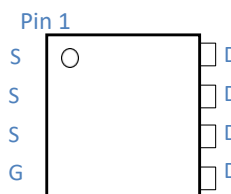
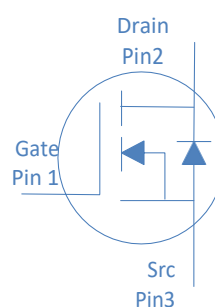
Application:

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

Part Number	Package	Marking
KPRGN035N08A	DFN5*6	廠別 GN035N08A / GN035N08A

V_{DS}	80	V
$R_{DS(on),typ}$	3	mΩ
I_D (Silicon Limited)	116	A
I_D (Package Limited)	60	A

DFN5*6



Absolute Maximum Ratings at $T_J=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current(Silicon Limited)	I_D	$T_C=25^\circ\text{C}$	116	A
		$T_C=100^\circ\text{C}$	73	
		$T_C=25^\circ\text{C}$	60	
Continuous Drain Current(Package Limited)				
Drain to Source Voltage	V_{DS}	-	80	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	400	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.1\text{mH}, T_C=25^\circ\text{C}$	80	mJ
Power Dissipation	P_D	$T_C=25^\circ\text{C}$	89	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	$^\circ\text{C}$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.4	$^\circ\text{C/W}$

Electrical Characteristics at $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	2.7	4.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=80V, T_j=25^{\circ}\text{C}$	-	-	1	μA
		$V_{GS}=0V, V_{DS}=80V, T_j=100^{\circ}\text{C}$	-	-	100	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	3	3.5	m Ω
Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$	-	65	-	S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$	-	1.20	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$	-	4347	-	pF
Output Capacitance	C_{oss}		-	703	-	
Reverse Transfer Capacitance	C_{rss}		-	28	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=40V, I_D=20A, V_{GS}=10V$	-	68	-	nC
Gate to Source Charge	Q_{gs}		-	13	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	17	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=20A, V_{GS}=10V, R_G=10\Omega,$	-	15	-	ns
Rise time	t_r		-	12	-	
Turn off Delay Time	$t_{d(off)}$		-	52	-	
Fall Time	t_f		-	19	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$V_R=40V, I_F=20A, dI_F/dt=100A/\mu s$	-	51	-	ns
Reverse Recovery Charge	Q_{rr}		-	61	-	nC

Fig 1. Typical Output Characteristics

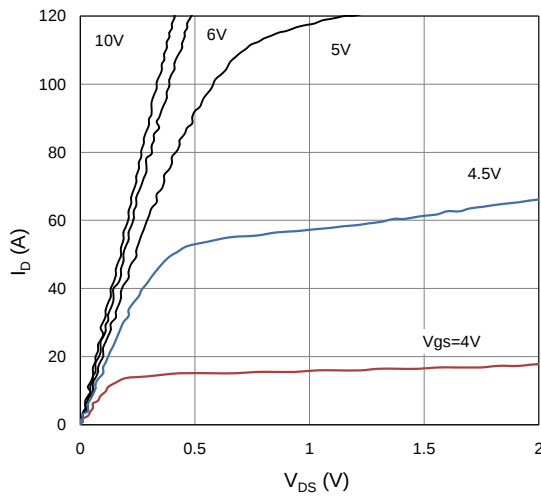


Figure 2. On-Resistance vs. Gate-Source Voltage

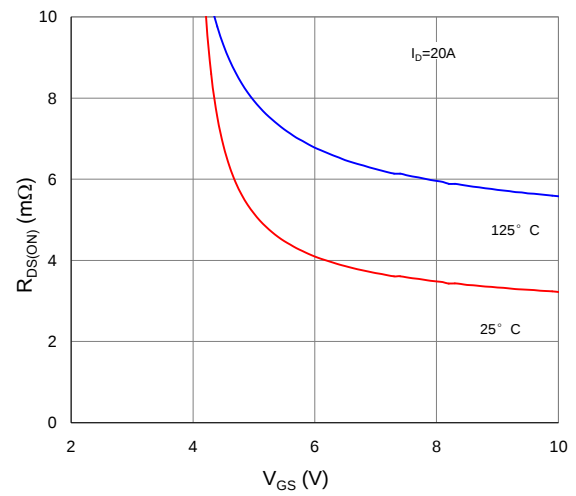


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

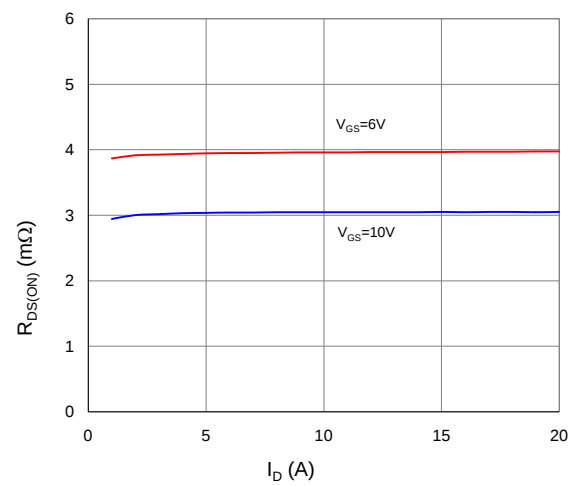


Figure 4. Normalized On-Resistance vs. Junction Temperature

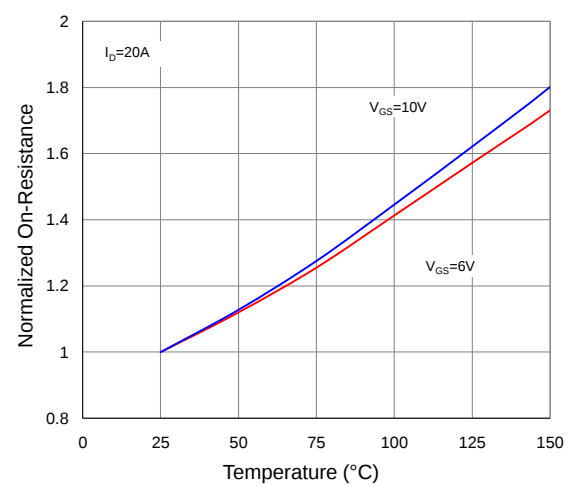


Figure 5. Typical Transfer Characteristics

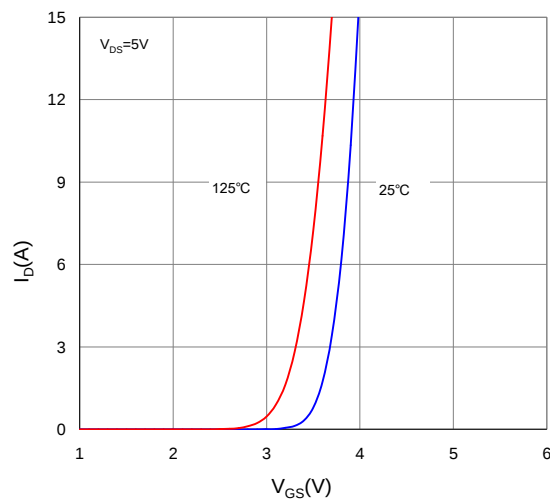


Figure 6. Typical Source-Drain Diode Forward Voltage

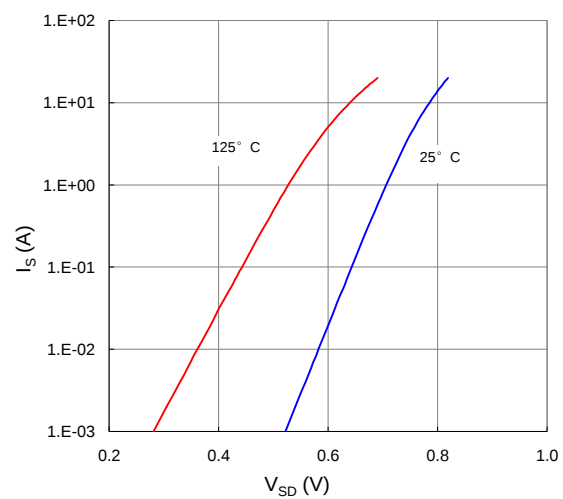


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

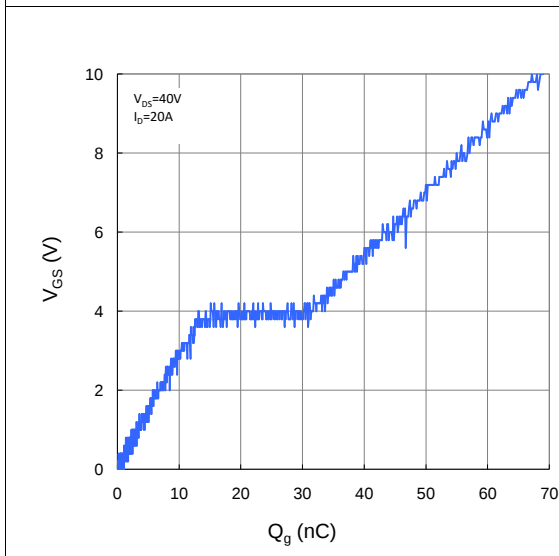


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

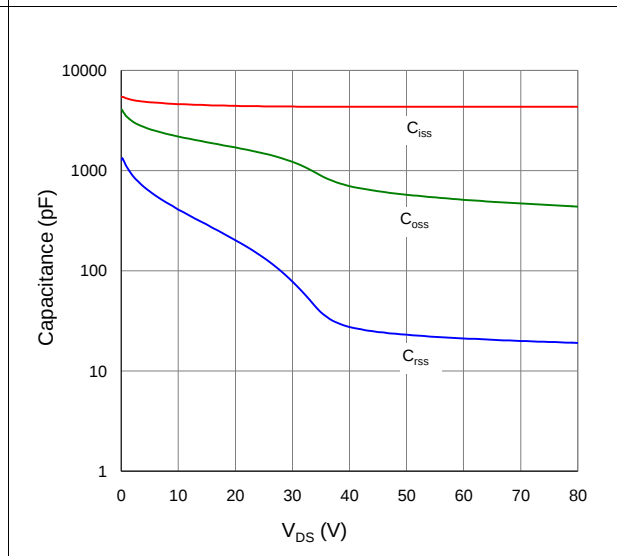


Figure 9. Maximum Safe Operating Area

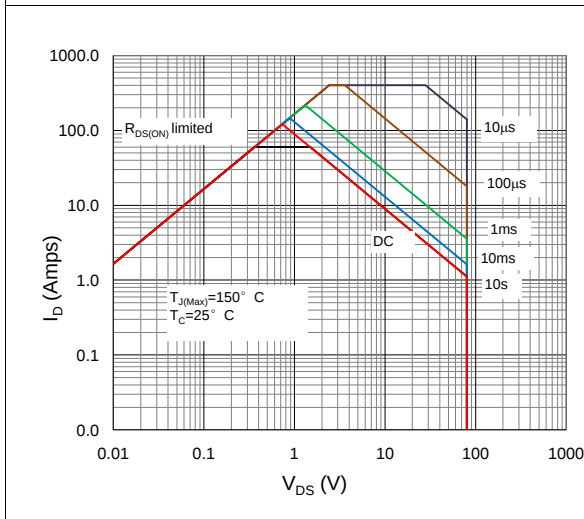


Figure 10. Maximum Drain Current vs. Case Temperature

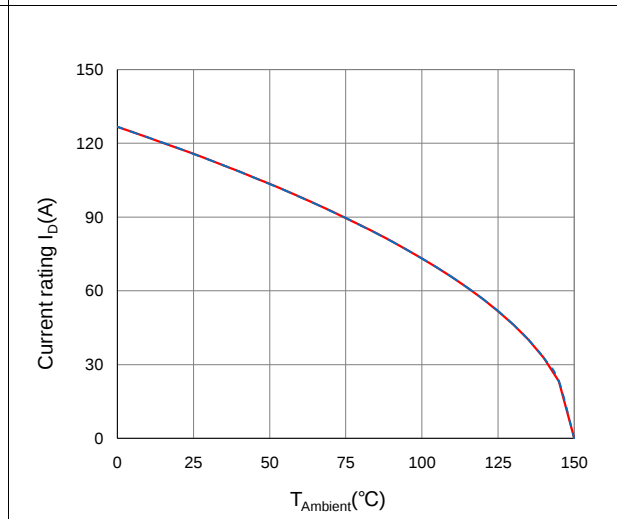
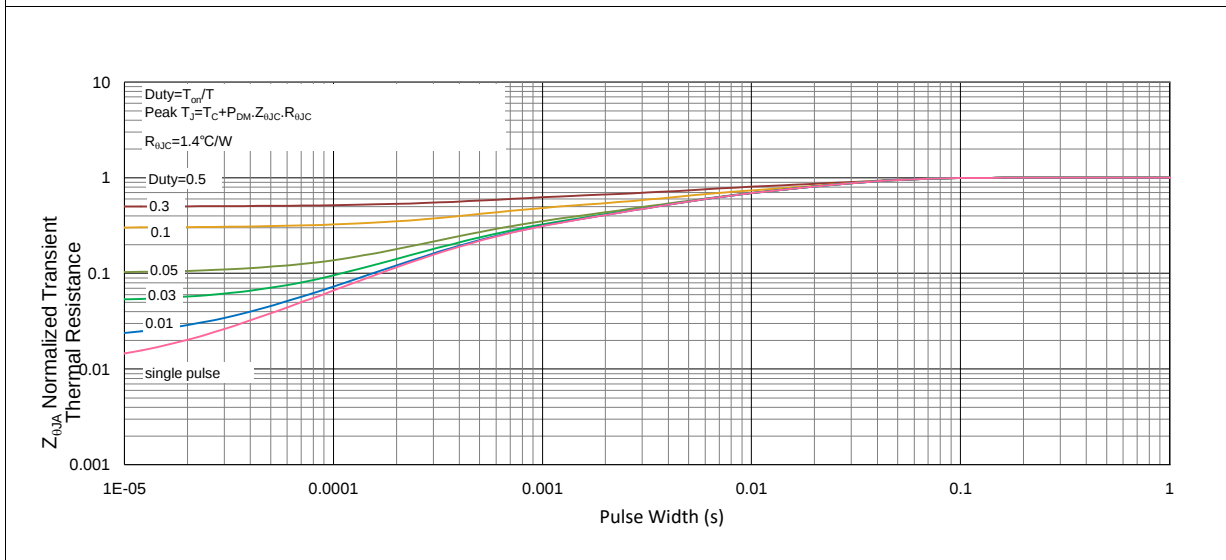
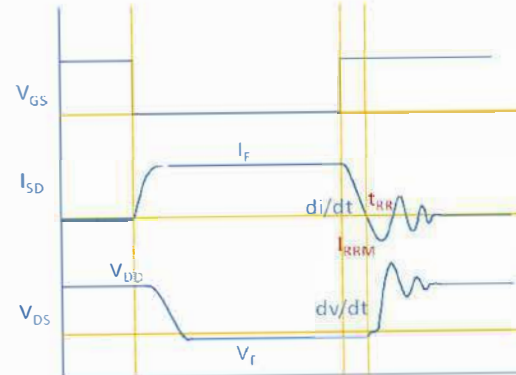
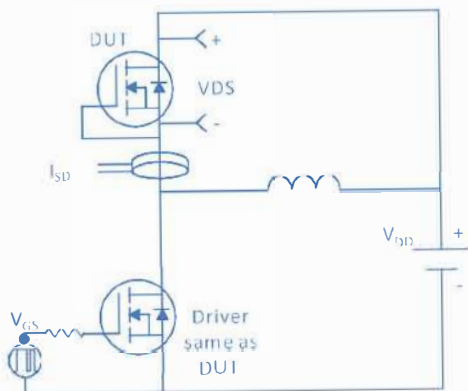
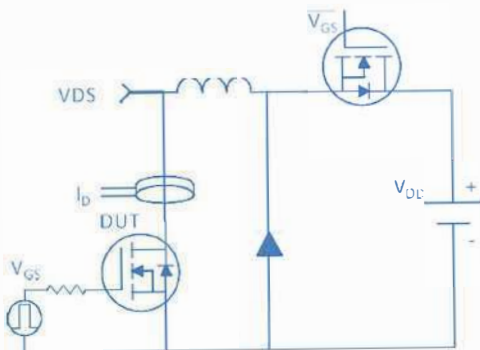
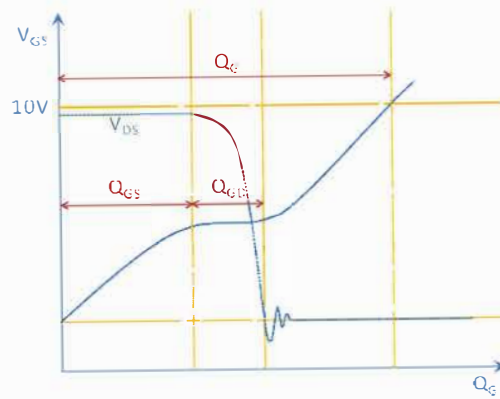
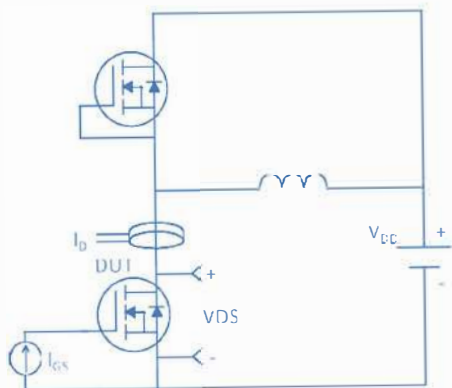
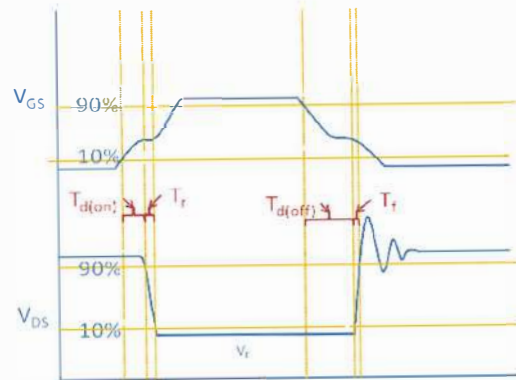
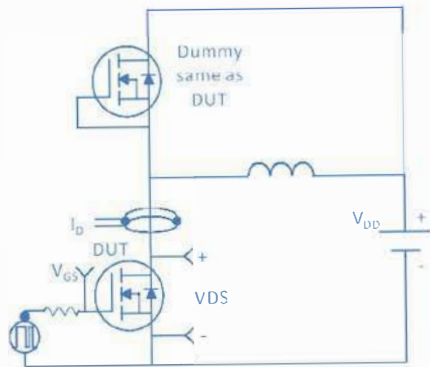


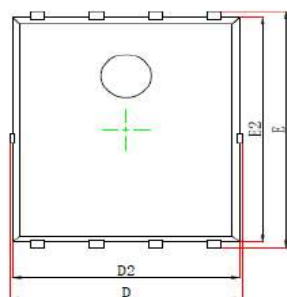
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



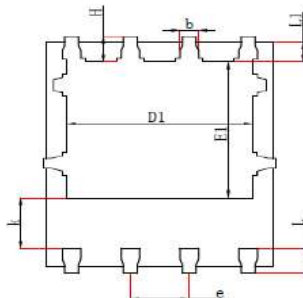


Package Outline

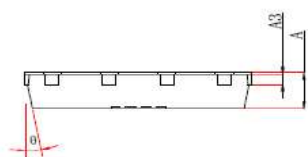
DFN5*6, 8 leads



Top View
[顶视图]



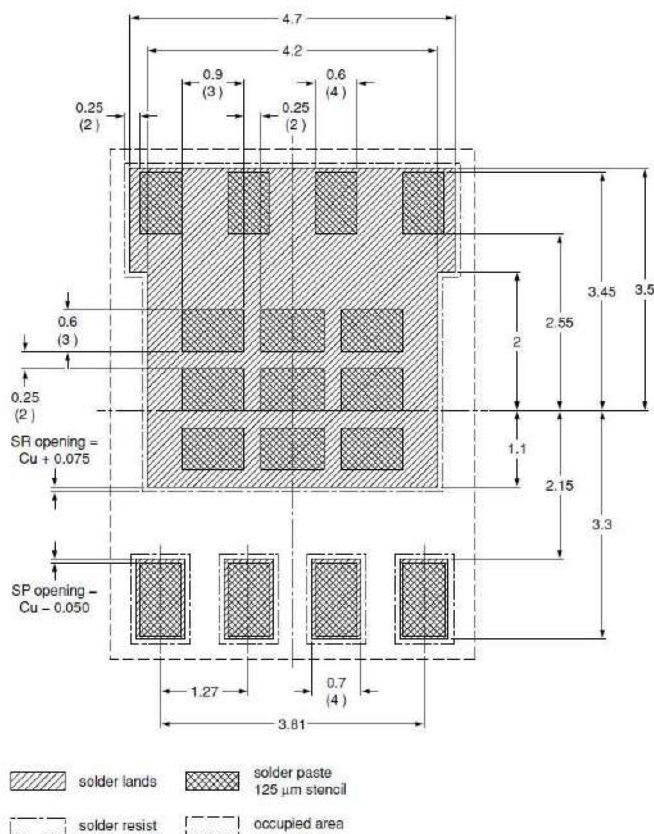
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A3	0.254 REF		0.010 REF	
D	4.680	5.120	0.184	0.202
E	5.900	6.126	0.232	0.241
D1	3.610	4.110	0.142	0.162
E1	3.380	3.780	0.133	0.149
D2	4.800	5.000	0.189	0.197
E2	5.674	5.826	0.223	0.229
k	1.100	1.390	0.043	0.055
b	0.330	0.510	0.013	0.020
e	1.270 TYP		1.270 TYP	
L	0.510	0.711	0.020	0.028
L1	0.424	0.576	0.017	0.023
H	0.410	0.726	0.016	0.029
θ	0°	12°	0°	12°

Recommended Soldering Footprint & Stencil Design



Taping Requirement 卷帶要求

1.1 Part's orientation shall be following in figure 1.

器件的方向必須如下圖 1。

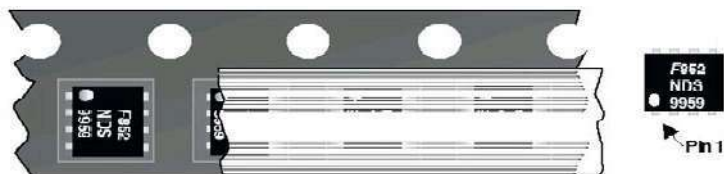


Figure 1

1.2 The quantity of per reel and per box shall be following in Figure 3 and Table 1. Including: Leaders, Trailers and Components.

每個卷帶盤和盒子的數量必須符合圖 2、表 1。包括：引頭，尾部和包裝數量。

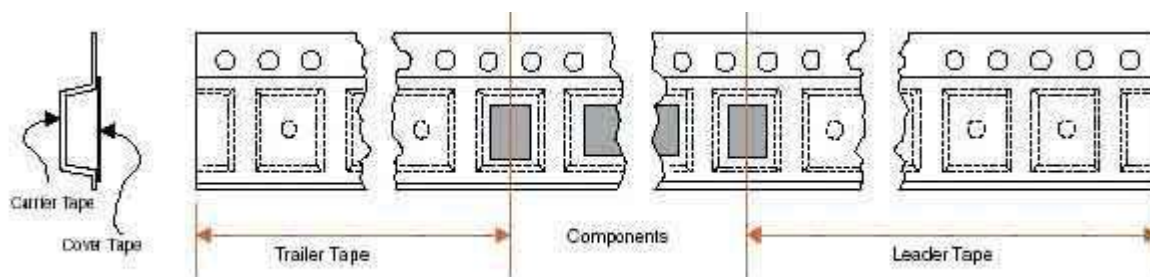


Figure 2

Trail(尾)	Leader(头)	Quantity/reel(数量/卷盘)
40±2 pockets(格)	65±2 pockets(格)	5 K