

80V N-Ch Power MOSFET

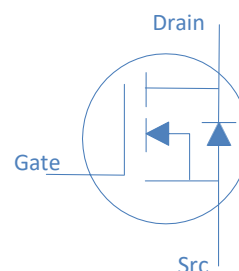
Features:

- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

Application:

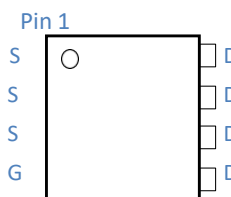
- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

DFN5*6



Part Number	Package	Marking
KPRGN028N08AL	DFN5*6	GN028N08AL

V_{DS}		80	V
$R_{DS(on),typ}$	$V_{GS}=10V$	2.5	m Ω
$R_{DS(on),typ}$	$V_{GS}=4.5V$	3.4	m Ω
I_D (Silicon Limited)		148	A
I_D (Package Limited)		60	A



Absolute Maximum Ratings at $T_J=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current(Silicon Limited)	I_D	$T_C=25^\circ\text{C}$	148	A
		$T_C=100^\circ\text{C}$	93	
		$T_C=25^\circ\text{C}$	60	
Continuous Drain Current(Package Limited)			60	
Drain to Source Voltage	V_{DS}	-	80	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	540	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.1\text{mH}, T_C=25^\circ\text{C}$	180	mJ
Power Dissipation	P_D	$T_C=25^\circ\text{C}$	119	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	$^\circ\text{C}$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.05	$^\circ\text{C/W}$

Electrical Characteristics at $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.7	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=80V, T_j=25^{\circ}\text{C}$	-	-	1	μA
		$V_{GS}=0V, V_{DS}=80V, T_j=100^{\circ}\text{C}$	-	-	100	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	2.5	3	$m\Omega$
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$	-	3.4	4.1	$m\Omega$
Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$	-	93	-	S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}\text{ Open}, f=1\text{MHz}$	-	0.4	-	Ω

Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$	-	4538	-	pF
Output Capacitance	C_{oss}		-	956	-	
Reverse Transfer Capacitance	C_{rss}		-	21	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=40V, I_D=20A, V_{GS}=10V$	-	105	-	nC
Total Gate Charge	$Q_g(4.5V)$		-	60	-	
Gate to Source Charge	Q_{gs}		-	13	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	32	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=20A, V_{GS}=10V$	-	18	-	ns
Rise time	t_r		-	11	-	
Turn off Delay Time	$t_{d(off)}$		-	40	-	
Fall Time	t_f		-	9	-	

Reverse Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=100A$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$V_R=40V, I_F=20A, dI_F/dt=100A/\mu s$	-	56	-	ns
Reverse Recovery Charge	Q_{rr}		-	68	-	nC

Fig 1. Typical Output Characteristics

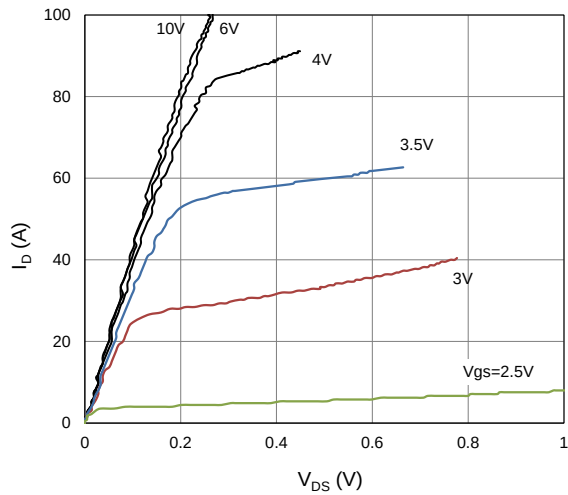


Figure 2. On-Resistance vs. Gate-Source Voltage

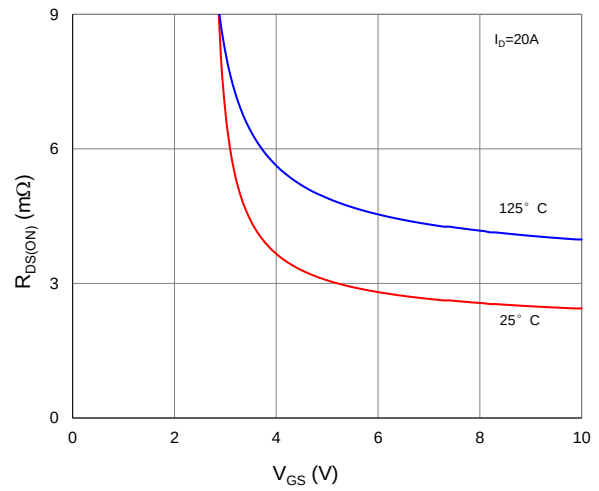


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

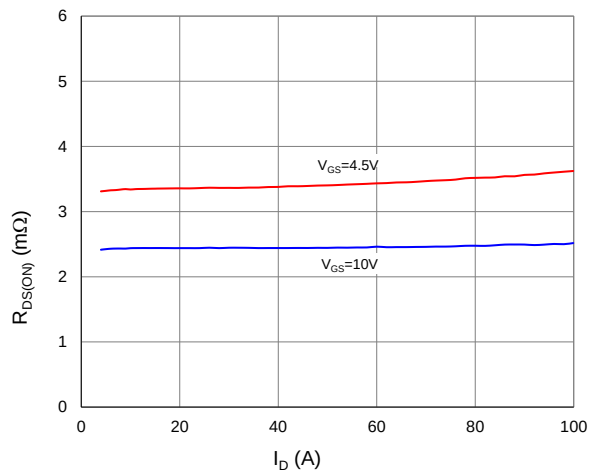


Figure 4. Normalized On-Resistance vs. Junction Temperature

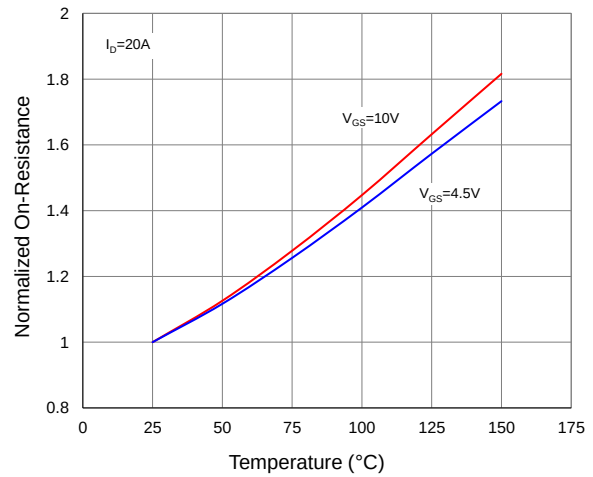


Figure 5. Typical Transfer Characteristics

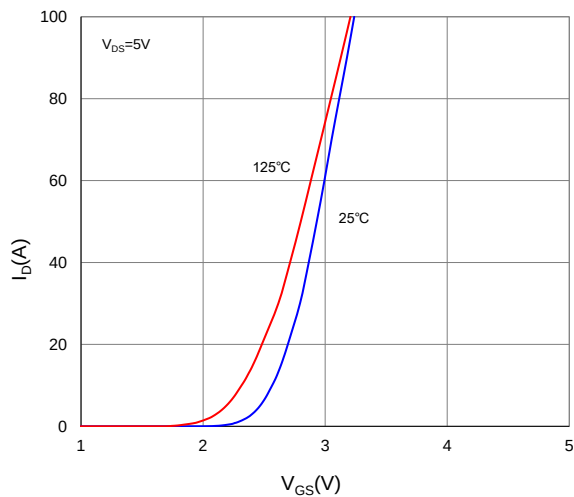


Figure 6. Typical Source-Drain Diode Forward Voltage

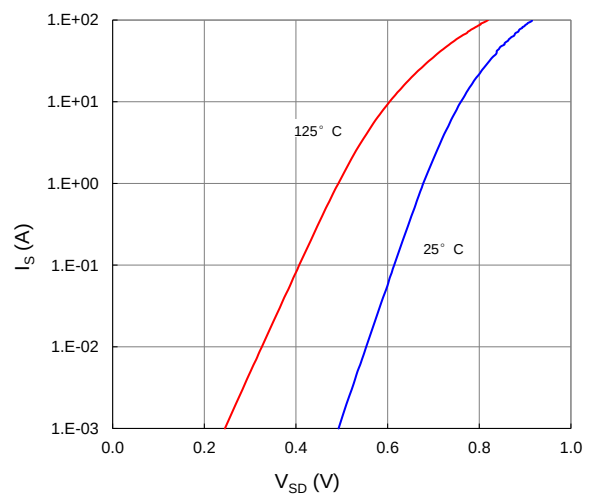


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

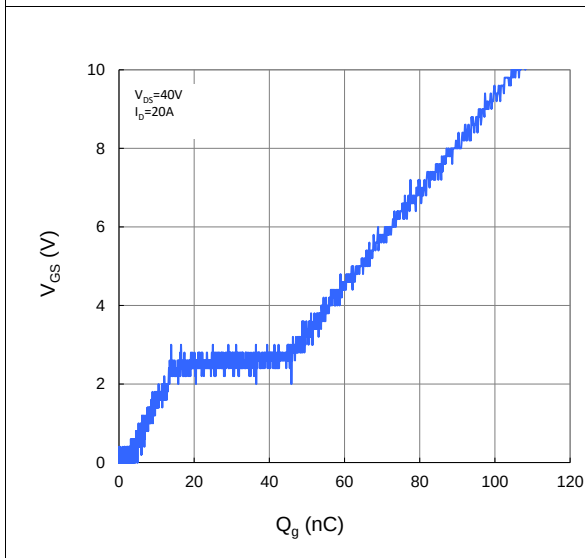


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

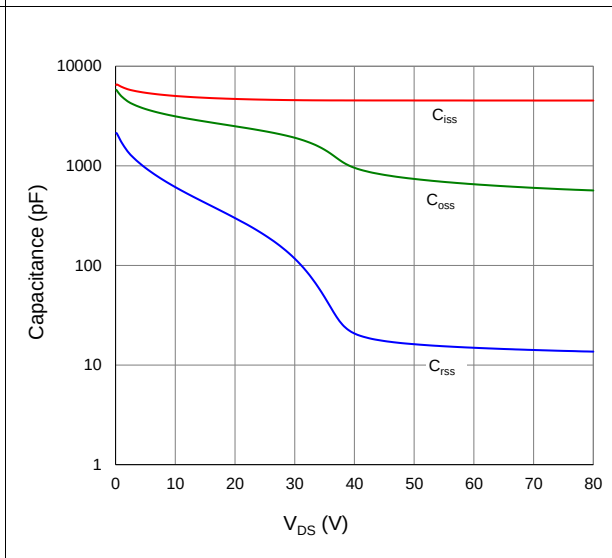


Figure 9. Maximum Safe Operating Area

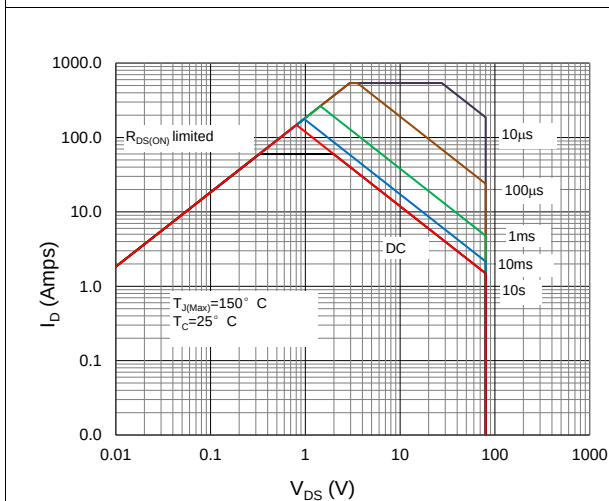


Figure 10. Maximum Drain Current vs. Case Temperature

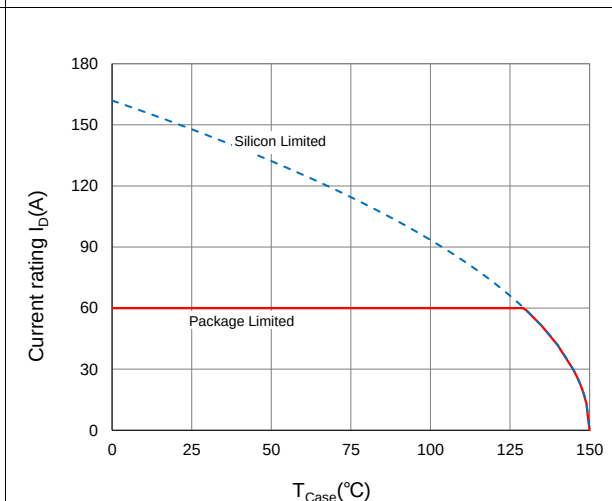
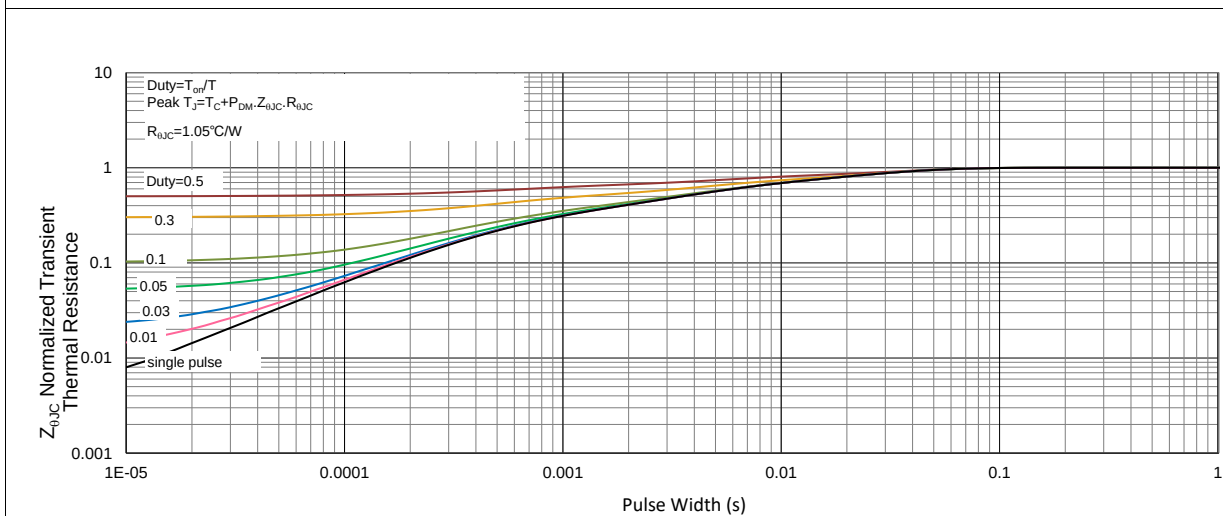
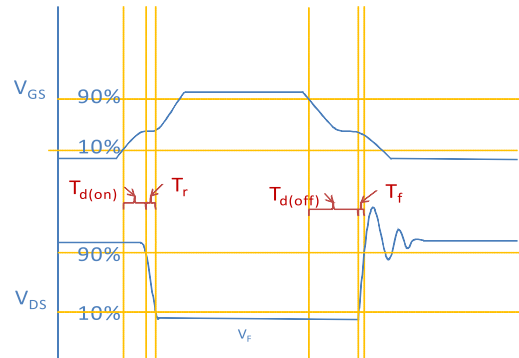
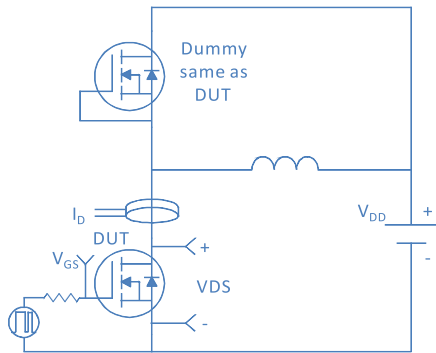


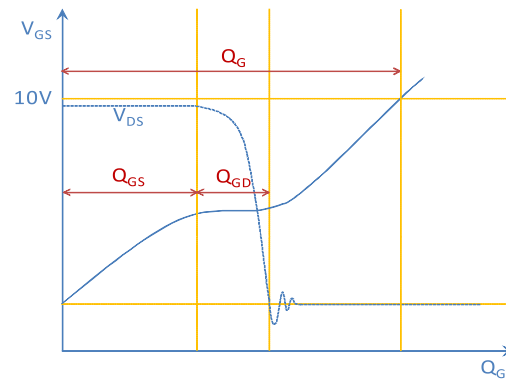
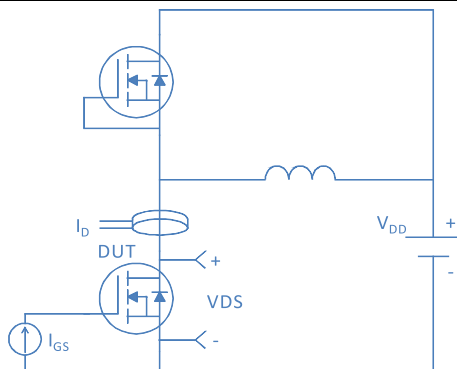
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



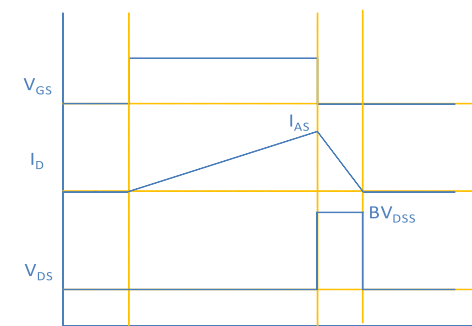
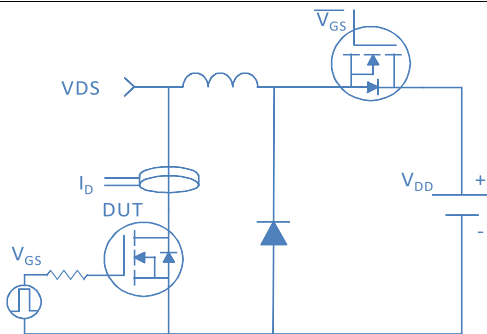
Inductive switching Test



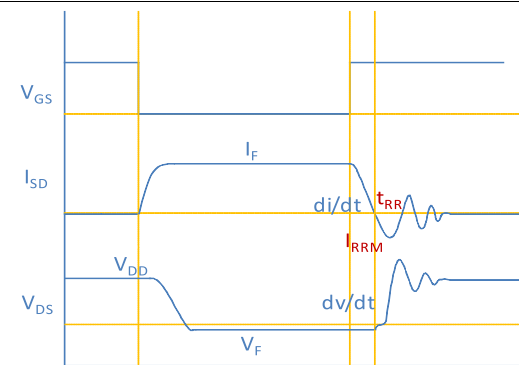
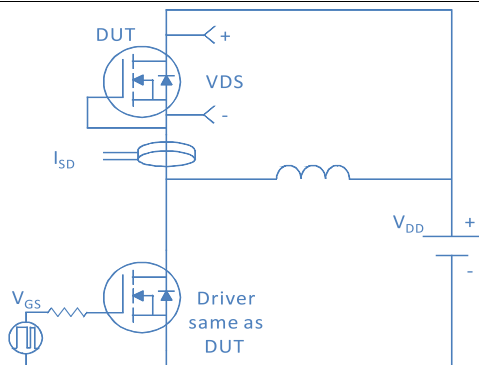
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

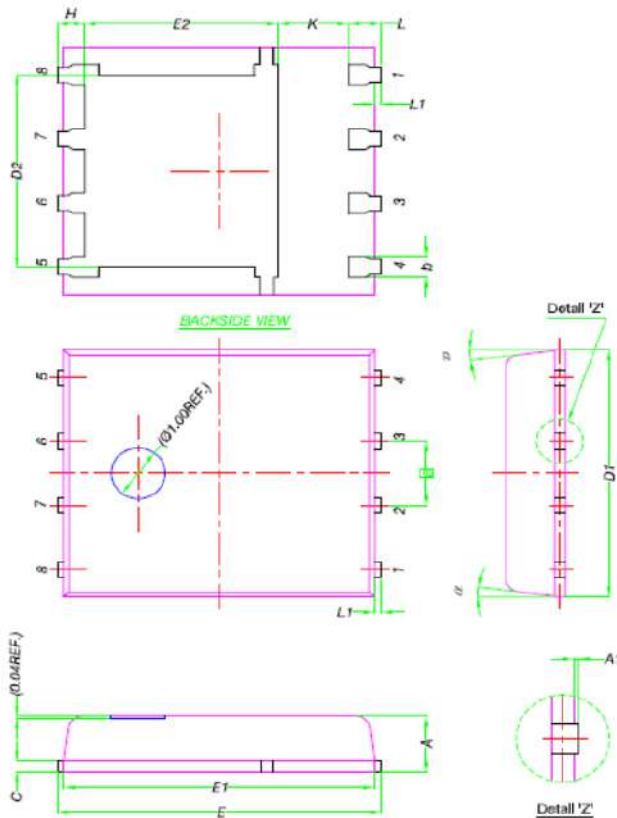


Diode Recovery Test



Package Outline

DFN5*6, 8 leads



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°