P-Ch 60V Fast Switching MOSFETs

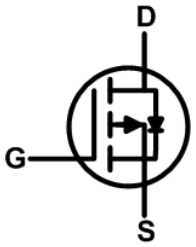
Features:

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

SOT223 Pin Configuration

Description:

The KWL6107 is the high cell density trenched P-ch MOSFETs, which provides excellent RDSON and efficiency for most of the small power switching and load switch applications. The KWL6107 meets the RoHS and Green Product requirement with full function reliability approved.



Product Summary

BVDSS	RDSON	ID
-60V	180mΩ	-2.3A

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-2.3	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ -10V[1]	-1.8	A
I_{DM}	Pulsed Drain Current[2]	-12	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	85	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	48	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-60	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.038	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-2A	---	140	180	mΩ
		V_{GS}=- 5V , I_D=-1.5A	---	200	260	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.5	-2.0	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.92	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-48V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-48V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-2A	---	5.3	---	S
Q_g	Total Gate Charge (-10V)	V_{DS}=-48V , V_{GS}=-10V , I_D=-2A	---	8.3	11.6	nC
Q_{gs}	Gate-Source Charge		---	1.8	2.52	
Q_{gd}	Gate-Drain Charge		---	1.6	2.25	
$T_{d(on)}$	Turn-On Delay Time	V_{DS}=-30V , V_{GS}=-10V , R_G=3.3Ω, I_D=-2A	---	4.1	8.2	ns
T_r	Rise Time		---	21	38	
$T_{d(off)}$	Turn-Off Delay Time		---	20.3	40.6	
T_f	Fall Time		---	21	42	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	428	600	pF
C_{oss}	Output Capacitance		---	39	55	
C_{rss}	Reverse Transfer Capacitance		---	26	36.4	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-2.3	A
I_{SM}	Pulsed Source Current[2,4]		---	---	-12	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

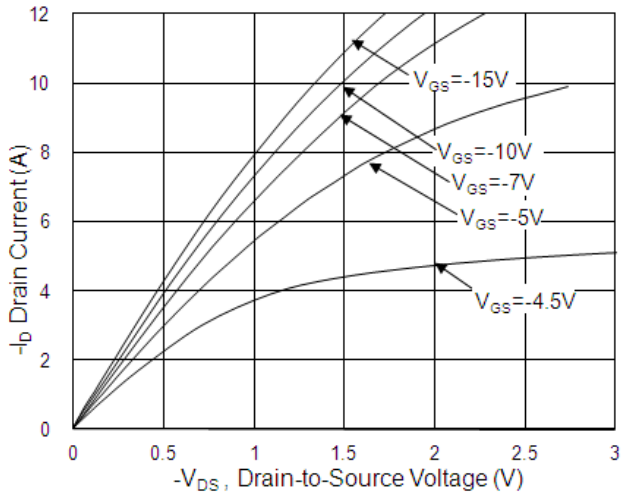


Fig.1 Typical Output Characteristics

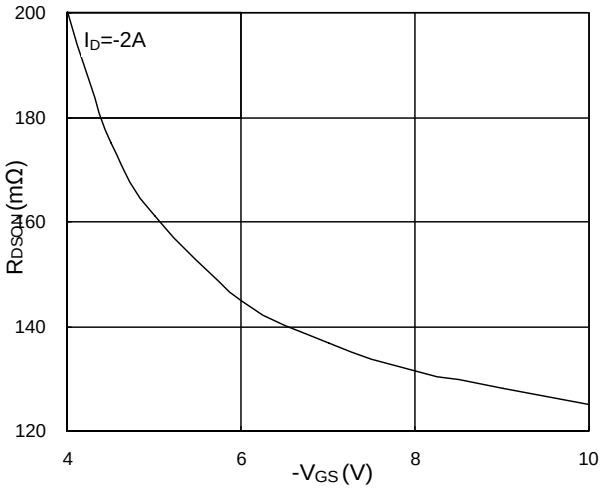


Fig.2 On-Resistance vs. Gate-Source Voltage

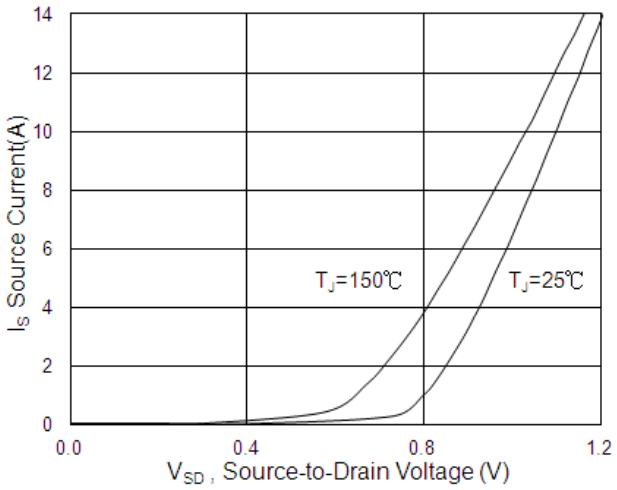


Fig.3 Forward Characteristics Of Reverse

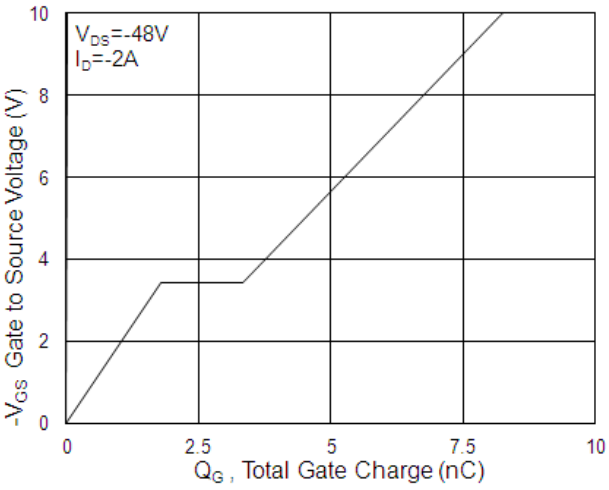


Fig.4 Gate-Charge Characteristics

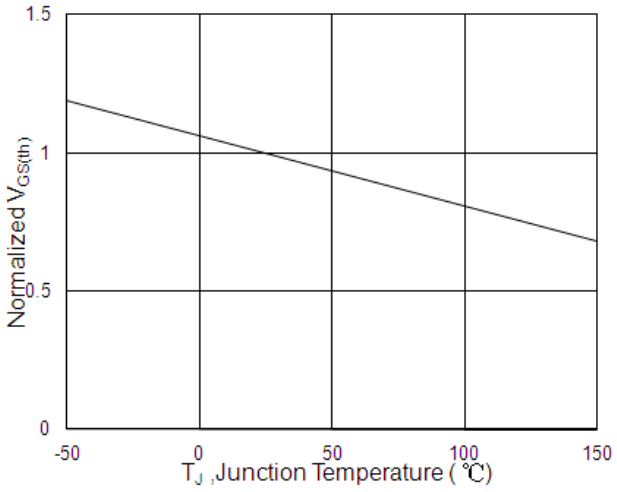


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

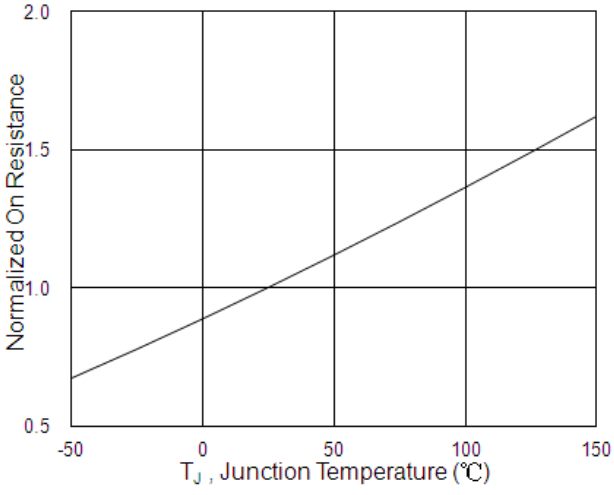


Fig.6 Normalized R_{DSON} vs. T_J

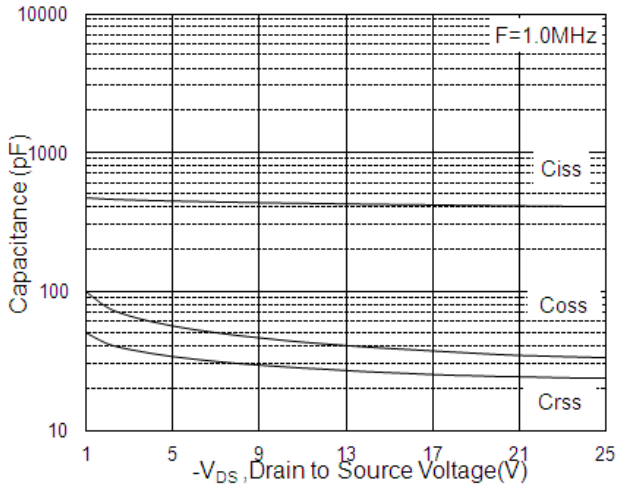


Fig.7 Capacitance

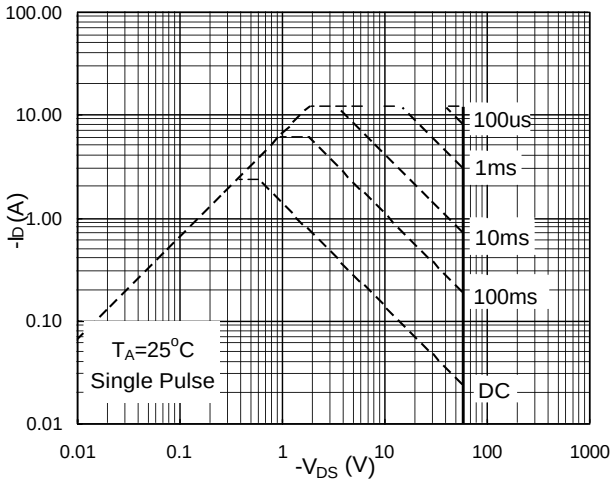


Fig.8 Safe Operating Area

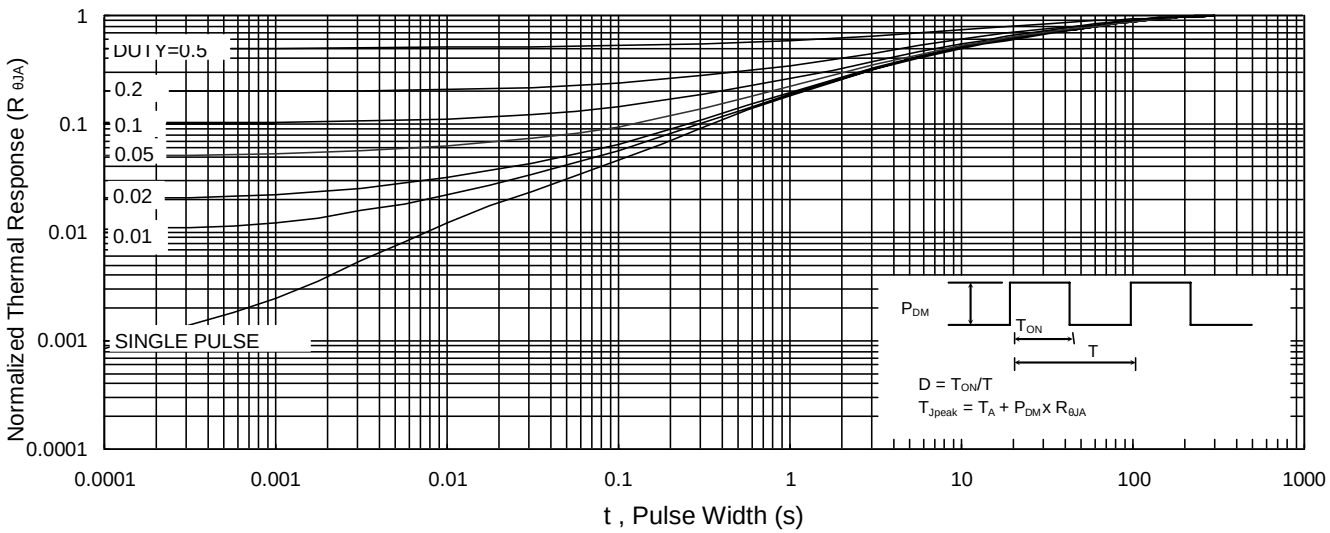


Fig.9 Normalized Maximum Transient Thermal Impedance

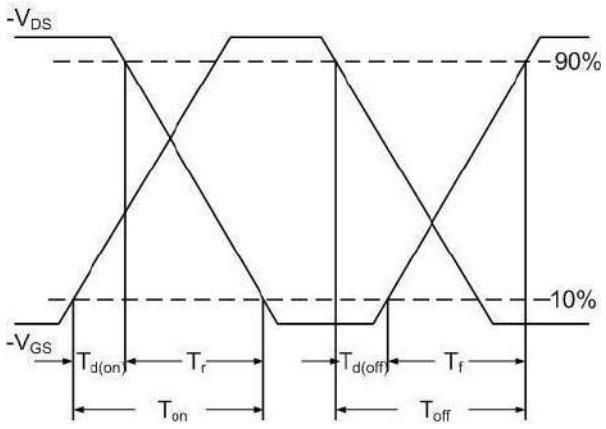


Fig.10 Switching time waveform

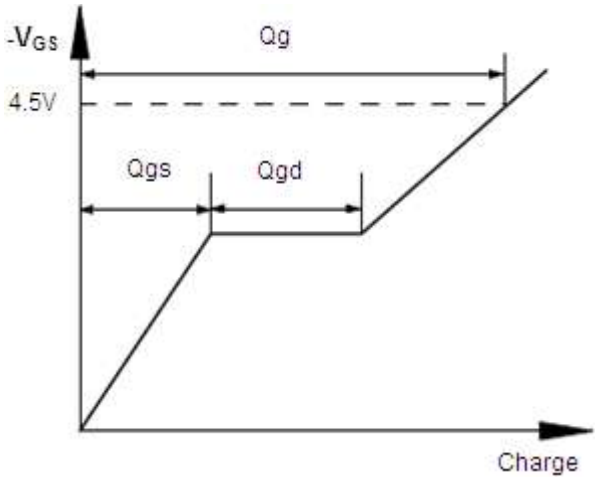


Fig.11 Gate Charge waveform