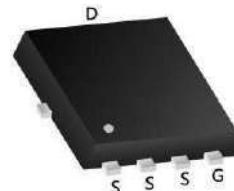


Single N-Channel MOSFET

Features:

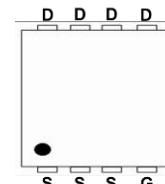
- Advanced Trench MOS Technology
- Low Gate Charge
- Low $R_{DS(ON)}$
- 100% EAS Guaranteed
- Green Device Available



PRPAK5X6 Pin Configuration

Applications:

- Motor Control.
- DC/DC Converter.
- Synchronous rectifier applications.



Product Summary

BVDSS	RDS(on)	ID
60V	8.5mΩ	58A

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current ^{1,6}	58	A
$I_D @ T_c=100^\circ C$		69 (Silicon limited)	A
I_D	Pulsed Drain Current ²	37	A
EAS	Single Pulse Avalanche Energy ³	250	mJ
I_{AS}	Avalanche Current	26.5	
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	23	mJ
T_{STG}	Storage Temperature Range	77	W
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹ ($t \leq 10S$)	---	25	°C/W
	Thermal Resistance Junction-ambient ¹ (Steady State)	---	60	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-case ¹	---	2.5	°C/W

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	60	---	---	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=15\text{A}$	---	7.0	8.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=15\text{A}$	---	10.5	12.5	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	---	2.3	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.3	---	Ω
Q_g	Total Gate Charge (10V)	$V_{\text{DS}}=30\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=15\text{A}$	---	15	---	nC
Q_{gs}	Gate-Source Charge		---	3.5	---	
Q_{gd}	Gate-Drain Charge		---	4.2	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=30\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$, $I_D=15\text{A}$	---	7	---	ns
T_r	Rise Time		---	4.5	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	26	---	
T_f	Fall Time		---	5	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=30\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1270	---	pF
C_{oss}	Output Capacitance		---	479	---	
C_{rss}	Reverse Transfer Capacitance		---	40	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,5,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	30	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=15\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$, $T_J=25^{\circ}\text{C}$	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	72	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. Single pulse width limited by junction temperature $T_{J(\text{MAX})}=150^{\circ}\text{C}$.
3. The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=23\text{A}$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
6. The maximum current rating is package limited.

Typical Characteristics

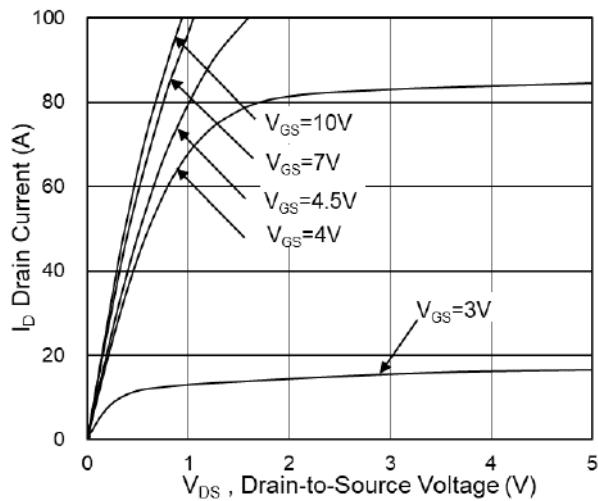


Fig.1 Typical Output Characteristics

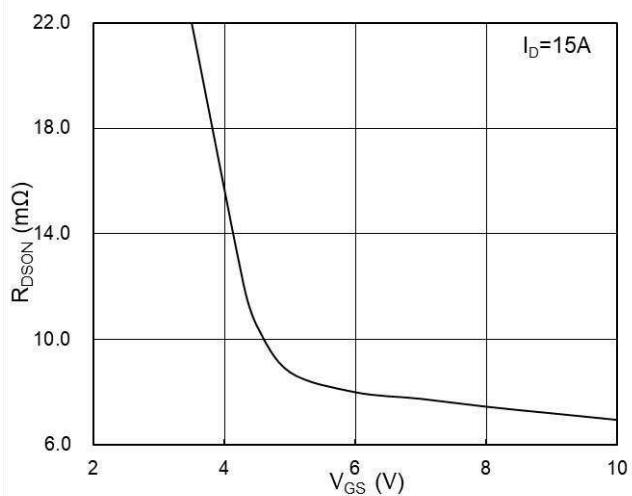


Fig.2 On-Resistance vs G-S Voltage

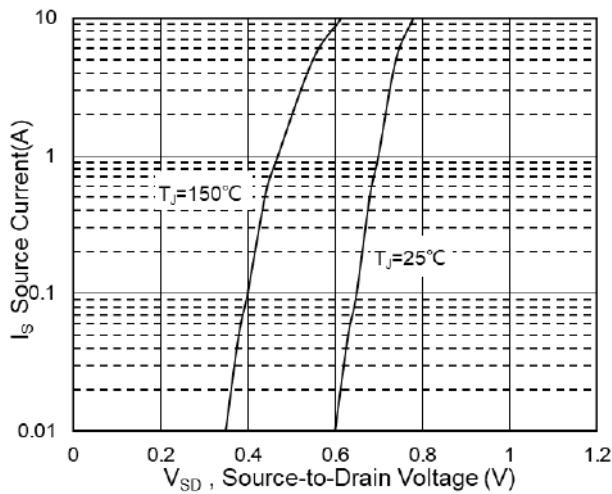


Fig.3 Source Drain Forward Characteristics

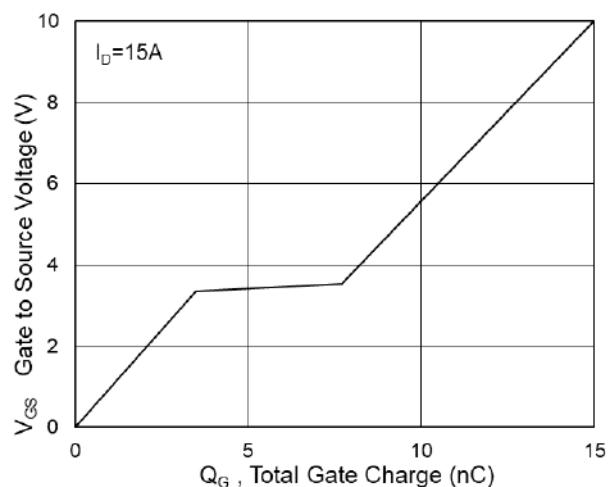


Fig.4 Gate-Charge Characteristics

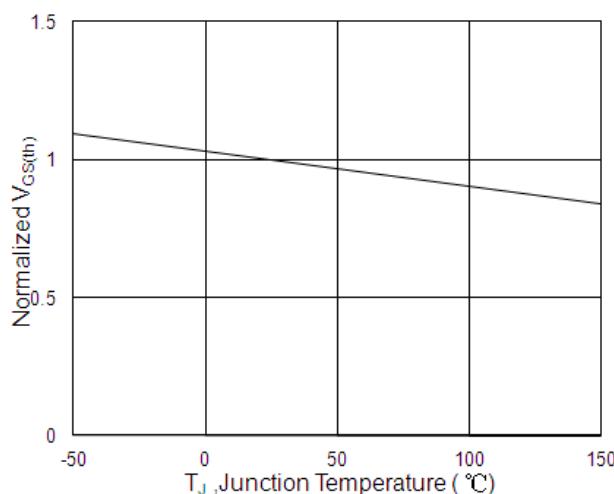


Fig.5 Normalized $V_{GS(th)}$ vs T_J

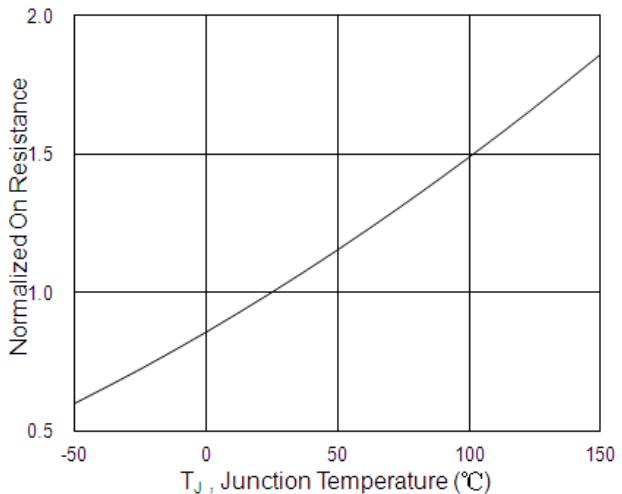


Fig.6 Normalized $R_{DS(on)}$ vs T_J

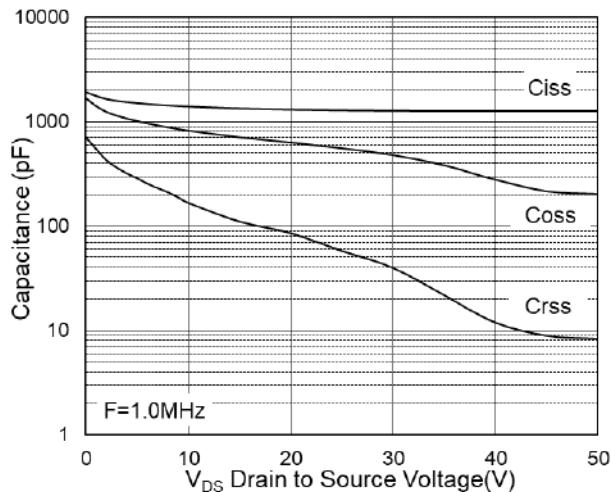


Fig.7 Capacitance

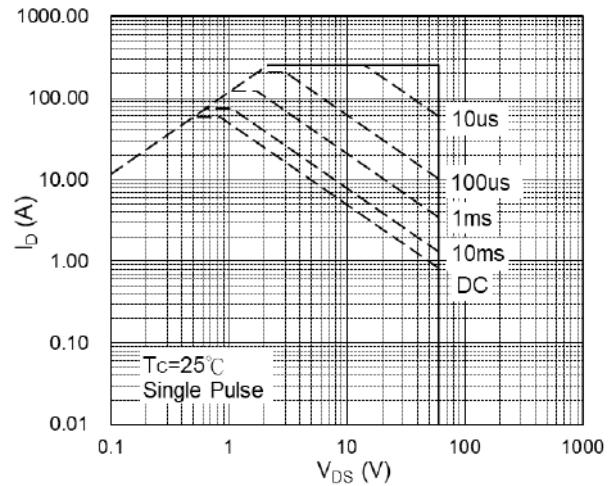


Fig.8 Safe Operating Area

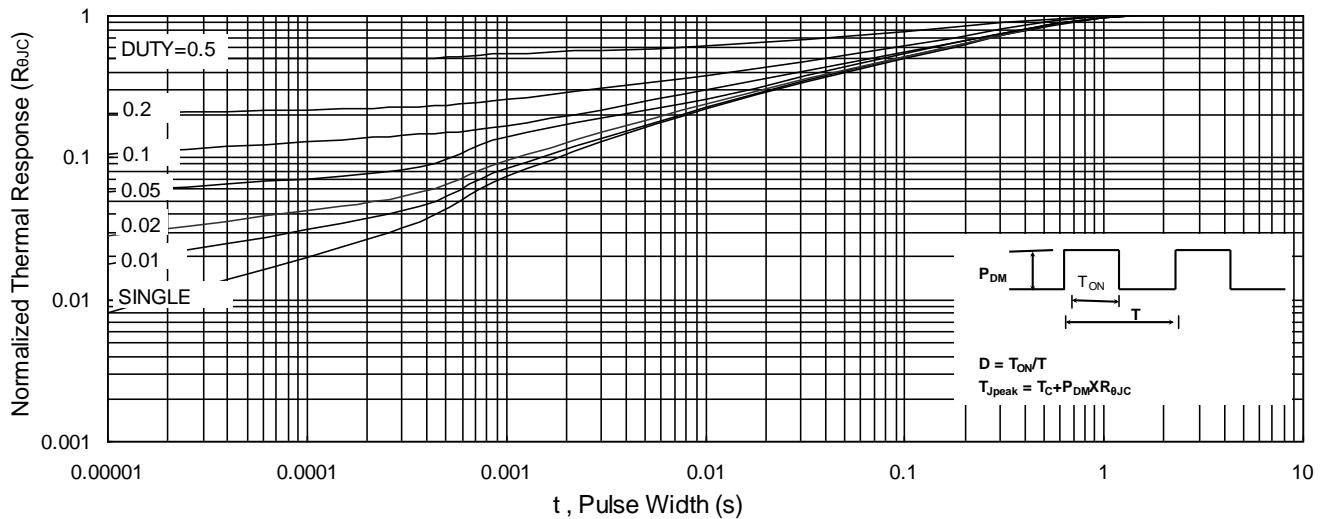


Fig.9 Normalized Maximum Transient Thermal Impedance

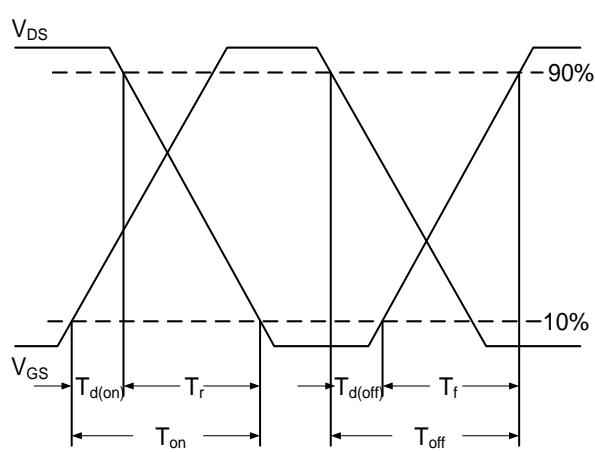


Fig.10 Switching Time Waveform

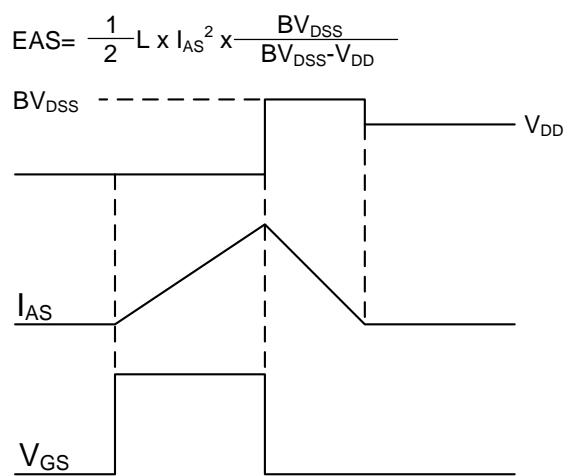


Fig.11 Unclamped Inductive Switching Waveform