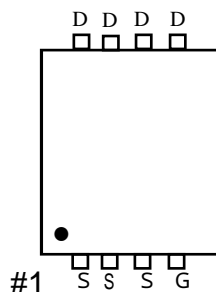


## N-Channel High Density Trench MOSFET

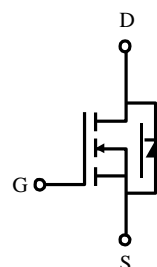
### Features:

- Super high dense cell trench design for low  $R_{DS(on)}$ .
- Rugged and reliable.
- Surface Mount package.



PDFN3333

PRODUCT SUMMARY		
$V_{(BR) DSS}$	$R_{DS(ON)}$	$I_D$
30V	13m $\Omega$	28A



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain current	$T_A = 25$	$I_D$	28	A
	$T_A = 100$		18	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	65	
Avalanche Current		$I_{AS}$	24	
Avalanche Energy	$L=0.1\text{mH}$	$E_{AS}$	22.5	mJ
Power Dissipation	$T_A = 25$	$P_D$	19.5	W
	$T_A = 100$		12.5	
Operating junction & Storage Temperature Range		$T_s$ $T_{stg}$	-55 to 150	

### THERMAL CHARACTERISTICS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta Jc}$		6	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.6	2.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =± V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0 V			1	μA
		V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, T <sub>J</sub> =125			30	
Drain-Source On- State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =16A		21	29	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =20A		13	18	
Forward Trans conductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =13A		12		S

**DYNAMIC**

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		1583		pF
Output Capacitance	C <sub>oss</sub>			181		
Reverse Transfer Capacitance	C <sub>rss</sub>			129		
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0V, f=1MHz		3.5		Ω
Total Gate Charge <sup>2</sup>	Q <sub>g(vgs=10V)</sub>	V <sub>DS</sub> =0.5V <sub>(BR)DSS</sub> , I <sub>D</sub> = A		29		nC
	Q <sub>g(vgs=4.5V)</sub>			14		
Gate Source Charge <sup>2</sup>	Q <sub>gS(VGS=10V)</sub>			2.8		
	Q <sub>gS(VGS=4.5V)</sub>			1.2		
Gate-Drain Charge <sup>2</sup>	Q <sub>gd(VGS=10V)</sub>			9.8		
	Q <sub>gd(VGS=4.5V)</sub>			7.1		
Turn-On Delay Time <sup>2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> =15V, R <sub>L</sub> =1.5Ω I <sub>D</sub> =20A, V <sub>GS</sub> =10V, R <sub>GS</sub> =6Ω		12		nS
Rise Time <sup>2</sup>	t <sub>r</sub>			24		
Turn-Off Delay Time <sup>2</sup>	t <sub>d(off)</sub>			37		
Fall Time <sup>2</sup>	t <sub>f</sub>			19		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>J</sub>=25 °C)**

Continuous Current	I <sub>S</sub>			1.3		A
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> =I <sub>S</sub> , V <sub>GS</sub> =0V		0.8		V
Reverse Recovery Time	T <sub>rr</sub>	I <sub>F</sub> =20V, dI <sub>F</sub> /dt=100A/μs		16		nS
Reverse Recovery Charge	Q <sub>rr</sub>			5.8		nC

Note

b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .

c. Independent of operating production testing .

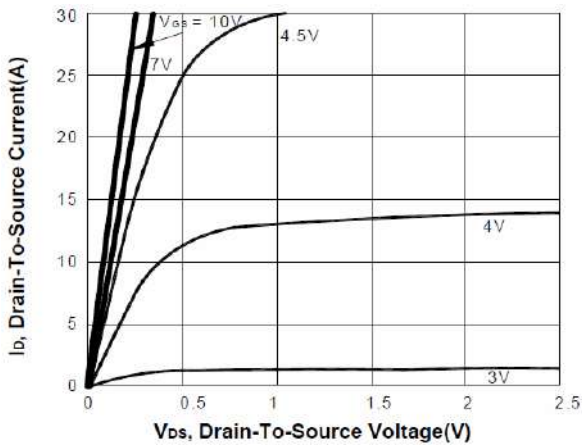


Figure 1. Output Characteristics

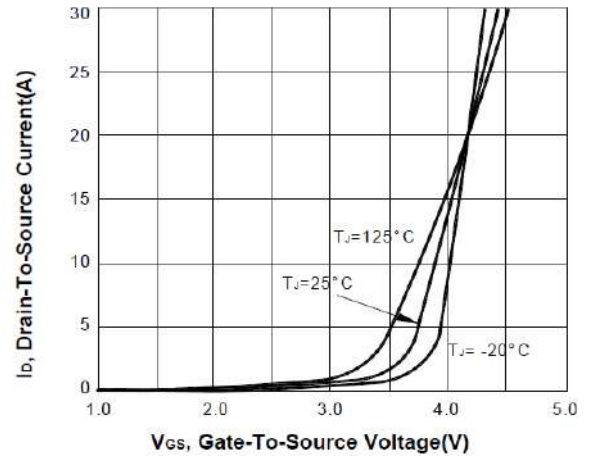


Figure 2. Transfer Characteristics

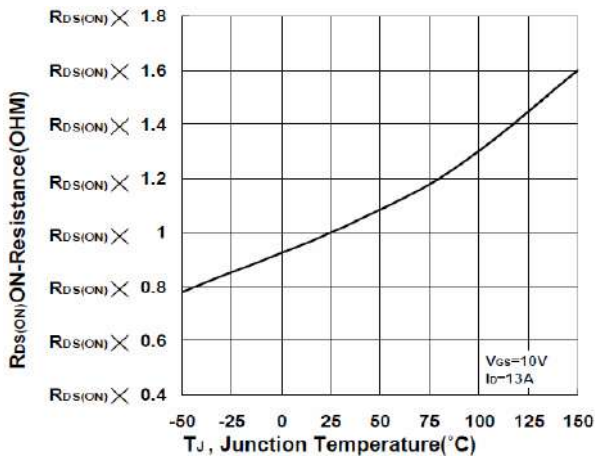


Figure 3. On-Resistance VS Temperature

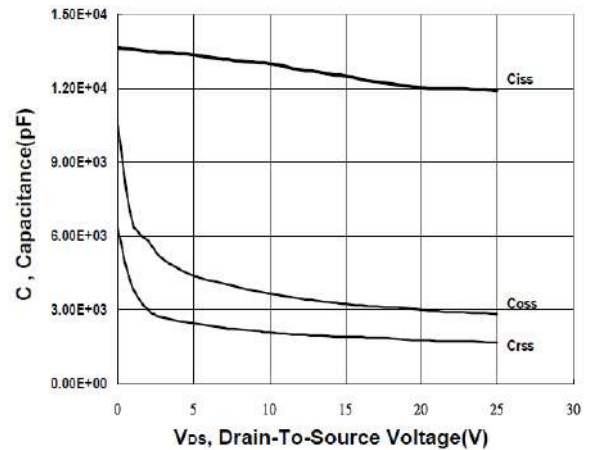


Figure 4. Capacitance Characteristic

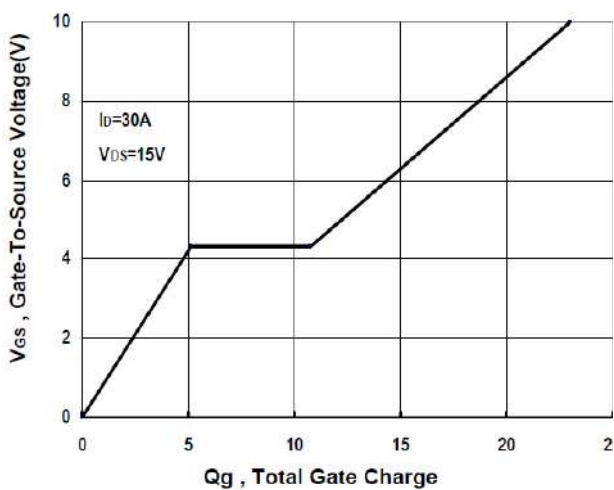


Figure 5. Gate charge Characteristics

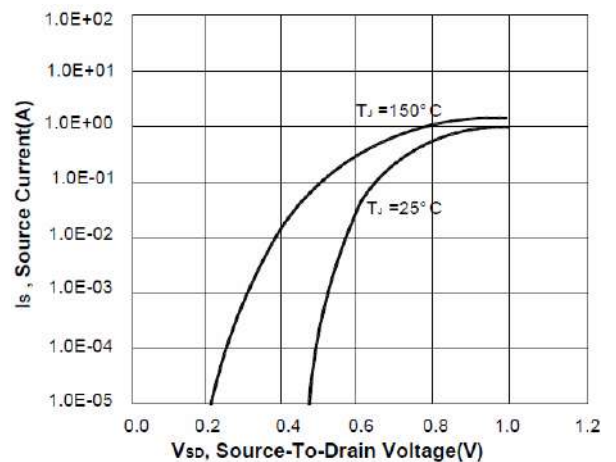


Figure 6. Source-Drain Diode Forward Voltage

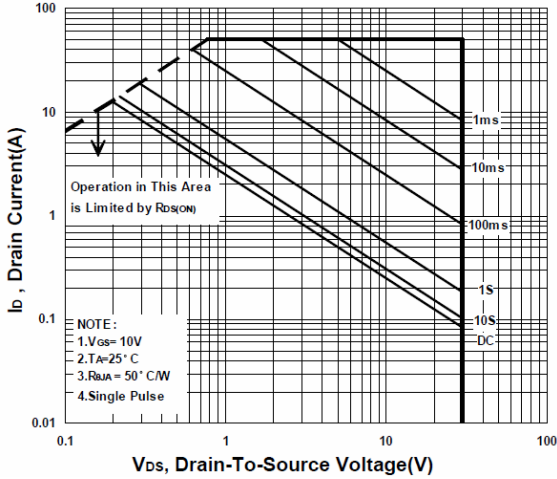


Figure 7. Safe Operating Area

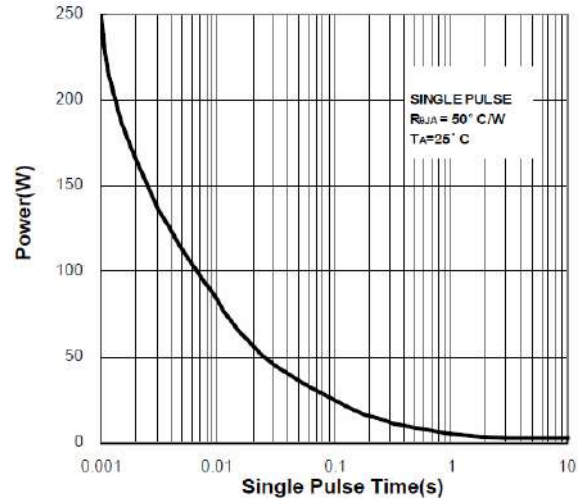


Figure 8 Single Pulse Maximum Power Dissipation

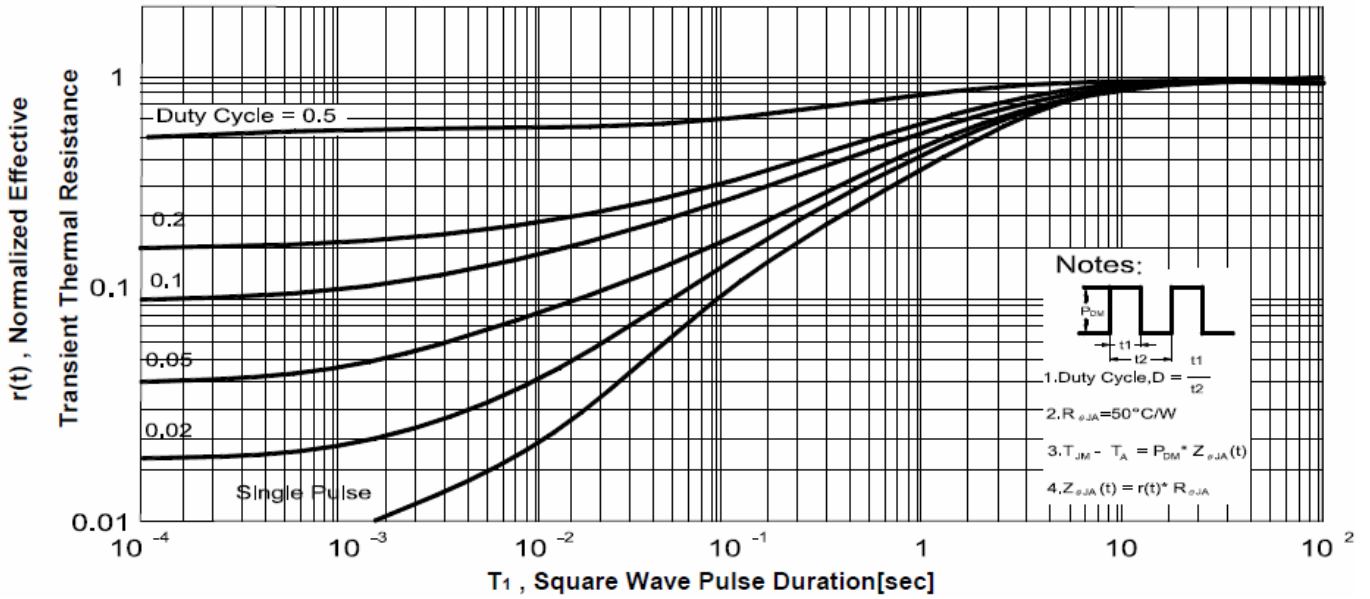


Figure 9. Transient Thermal Response Curve