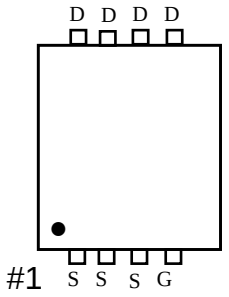
N-Channel High Density Trench MOSFET

Features:

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.



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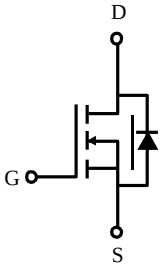


PRODUCT SUMMARY		
$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
30V	4mΩ	72A

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAME TERS TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gata-Source voltage		V_{GS}	±20	V
Continuous Drain current	T_C = 25℃	I_D	72	A
	T_C = 100 ℃		50	
Puised Drain Current[1]		I_{DM}	180	
Avalanche Current		I_{AS}	20	
Avalanche Energy	L=0.1mH	E_{AS}	25	mJ
Power Dissipation	T_C = 25 ℃	P_D	32	W
	T_C = 100 ℃		14	
Operaing junction & Storege Temperature Range		T_s,T_{stg}	-55 to 150	℃

THERMAL CHARACTERISTICS

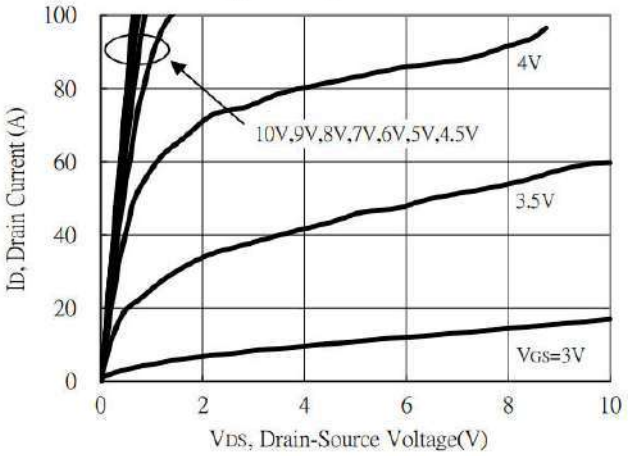
THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta Jc}$		4.5	℃/W
Junction-to-Ambient	$R_{\theta JA}$		54	℃/W

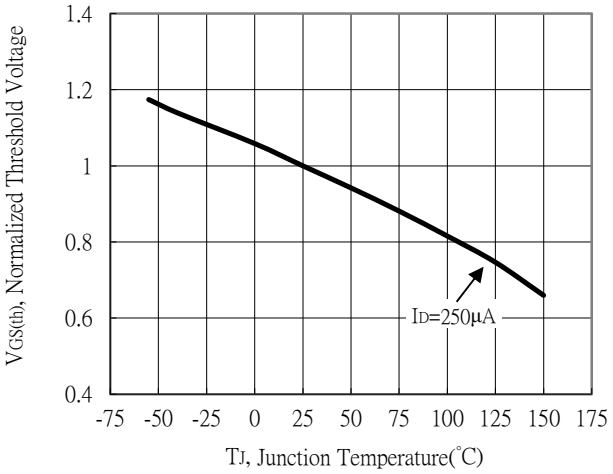
ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

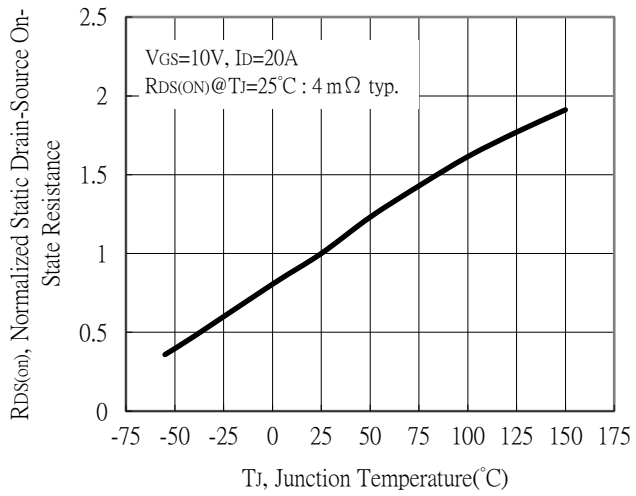
PARAMETER	SYNBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltege	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	1.6	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS}=0V,V_{GS}=± 20V			±100	nA
Zero Gate Voltage Dain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0 V			1	μA
		V_{DS}=20V,V_{GS}=0V,T_J=125 ℃			30	μA
Drain-Source On- State Resistance[1]	$R_{DS(ON)}$	V_{GS}=4.5V,I_D=16A		5.2	7.2	mΩ
		V_{GS}=10V,I_D=20A		4	6	mΩ
Forward Trans conductance[1]	g_{fs}	V_{DS}=5V,I_D=13A		22		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=15V,f=1MHz		1860		pF
Output Capacitance	C_{oss}			260		pF
Reverse Transfer Capacitance	C_{rss}			212		pF
Gate Resistance	R_G	V_{GS}=0V,f=1MHz		2.2		Ω
Total Gate Charge[2]	$Q_{g(vgs=10V)}$	V_{DS}=15V (BR)DSS, I_D = 20A		48		nC
	$Q_{g(vgs=4.5V)}$			26		nC
Gate Source Charge[2]	$Q_{gS(VGS=10V)}$			3.4		nC
	$Q_{gS(VGS=4.5V)}$			2.8		nC
Gate-Drain Charge[2]	$Q_{gd(VGS=10V)}$			14		nC
	$Q_{gd(VGS=4.5V)}$			9		nC
Tum-On Delay Time[2]	$t_{d(on)}$	V_{DS}=15V,R_L=1.5Ω I_D=20A,V_{GS}=10V.R_{GS}=6Ω		9.6		nS
Rise Time[2]	t_r			23.4		nS
Tum-Off Delay Time[2]	$t_{d(off)}$			62.8		nS
Fall Time[2]	t_r			23		nS
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS(T_J=25℃)						
Continuous Current	I_S			38		A
Forward Voltage[1]	V_{SD}	I_F=I_S,V_{GS}=0V		0.75	1.1	V
Reverse Recovery Time	T_{rr}	I_F=20V,d_{1f}/d_t=100A/μs		18.2		nS
Reverse Recovery Charge	Q_{rr}			9.2		nC

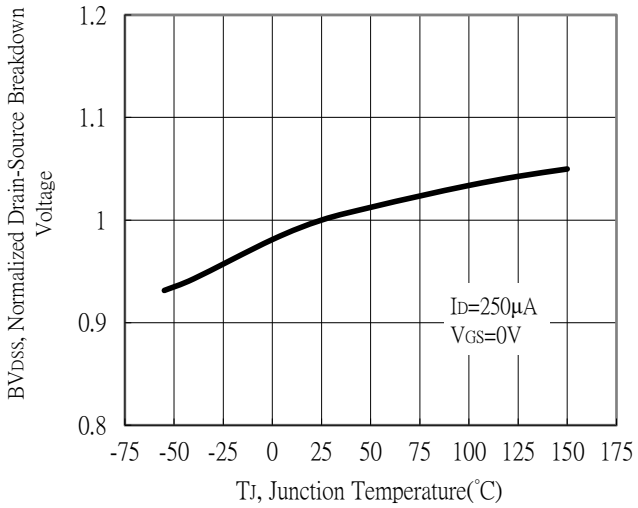
Note
b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .
c. Independent of operating production testing .

Typical Output Characteristics

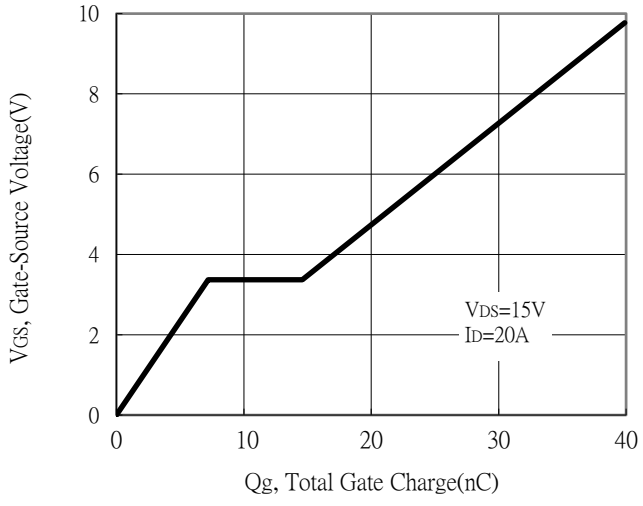


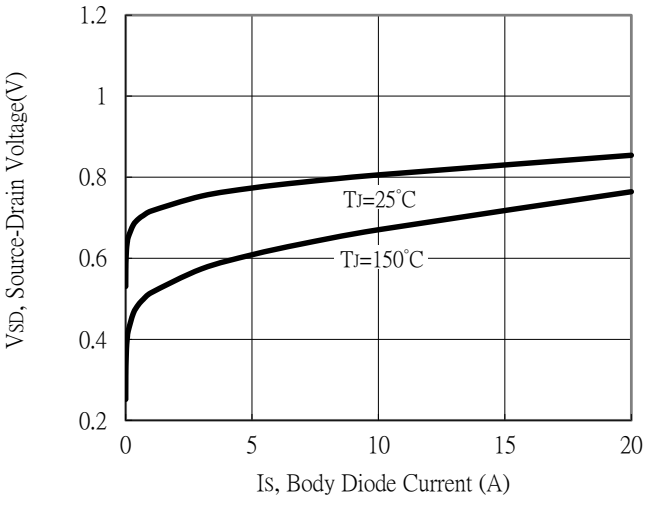




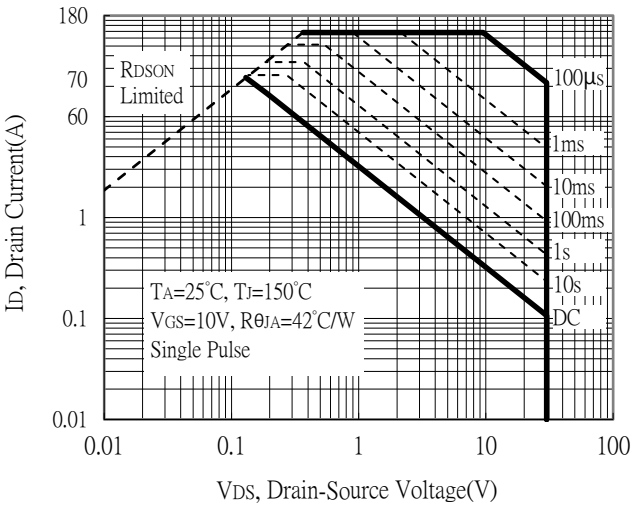


Gate Charge Characteristics

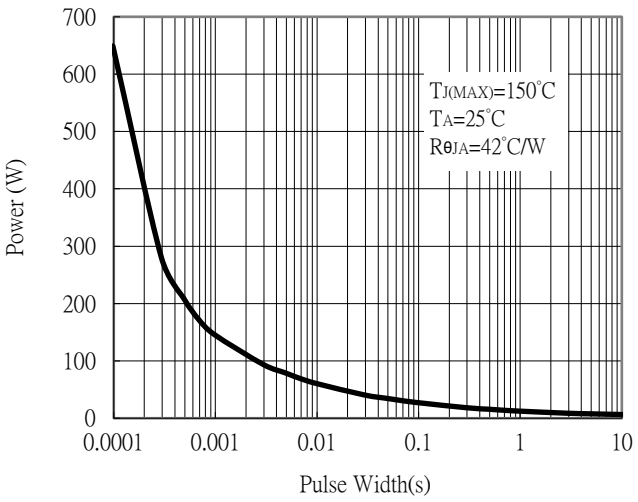




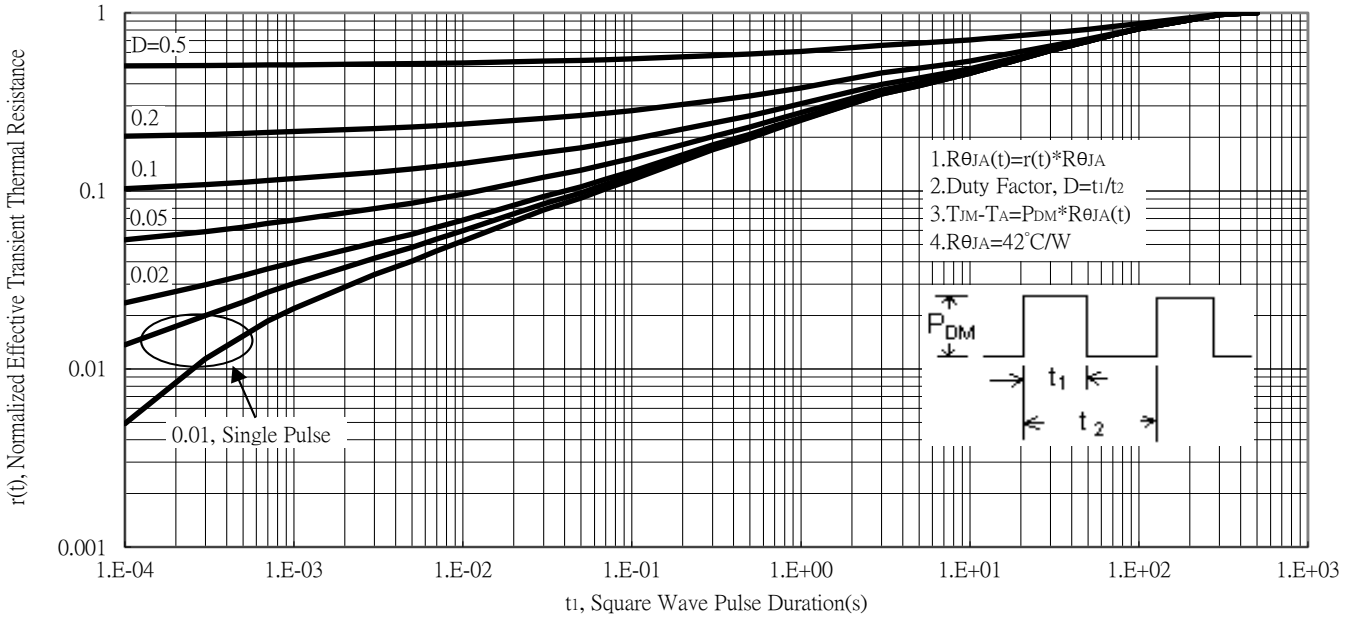
Maximum Safe Operating Area

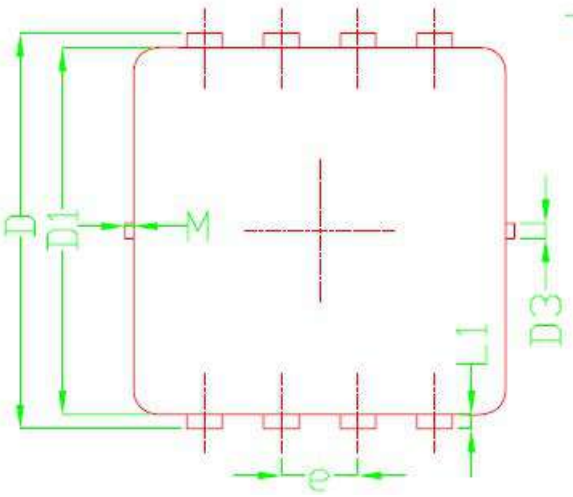


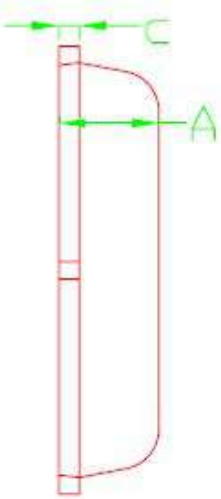
Single Pulse Power Rating, Junction to Ambient

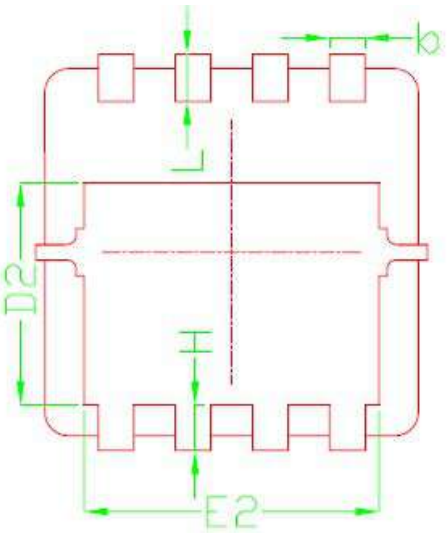


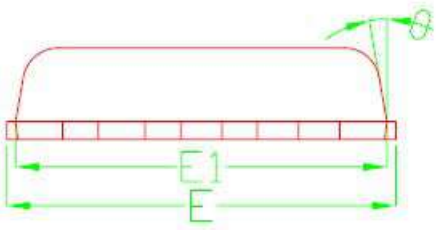
Transient Thermal Response Curves

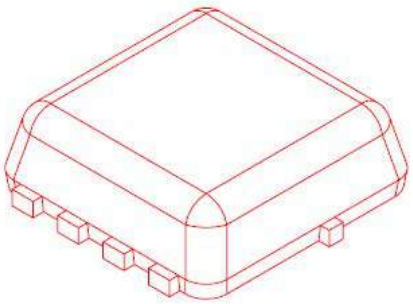




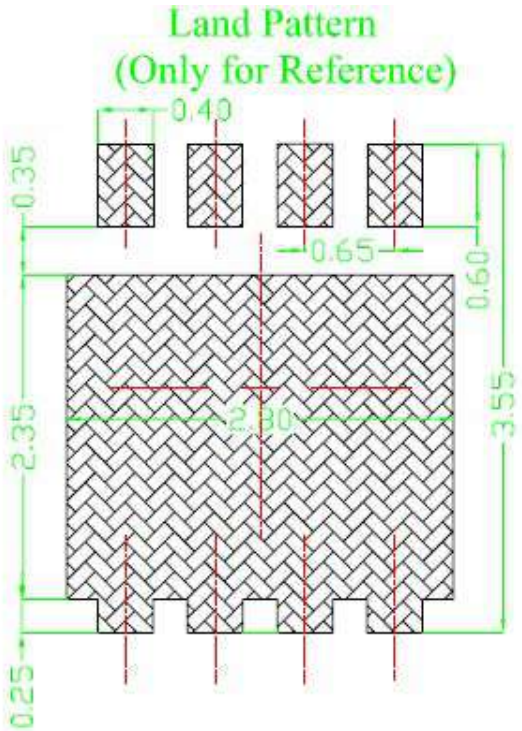








SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.
   Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body
   Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash,
   But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.