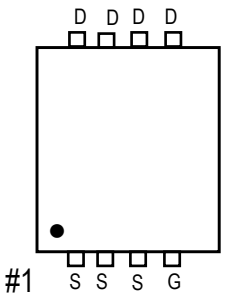
N-Channel High Density Trench MOSFET

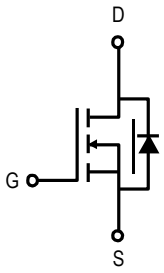
Features:

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

PDFN5x6



PRODUCT SUMMARY		
$V_{(BR)DSS}$	$R_{DS(ON)}$	ID
60V	7m Ω	38A



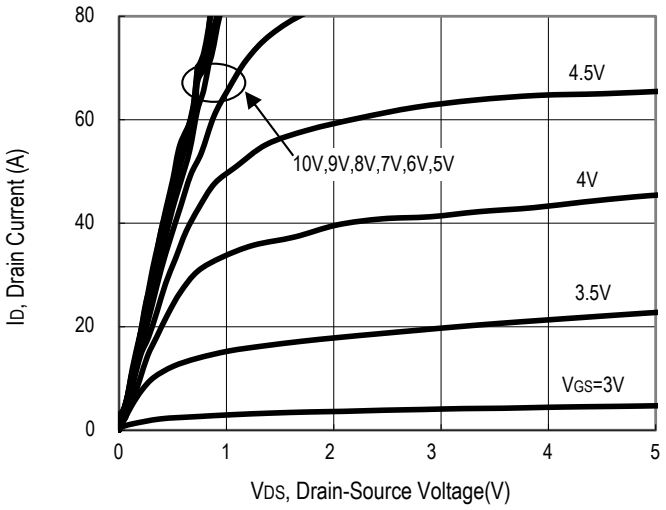
PARAME TERS TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gata-Source voltage		VGS	±20	V
Continuous Drain current	TC = 25℃	ID	38	A
	TC = 100 ℃		27	
Puised Drain Current[1]		IDM	140	
Avalanche Current		IAS	21	
Avalanche Energy	L=0.5mH	EAS	56	mJ
Power Dissipation	TC = 25 ℃	PD	36	W
	TC = 100 ℃		15	
Operaing junction & Storege Temperature Range		Ts,Tstg	-55 to 150	℃

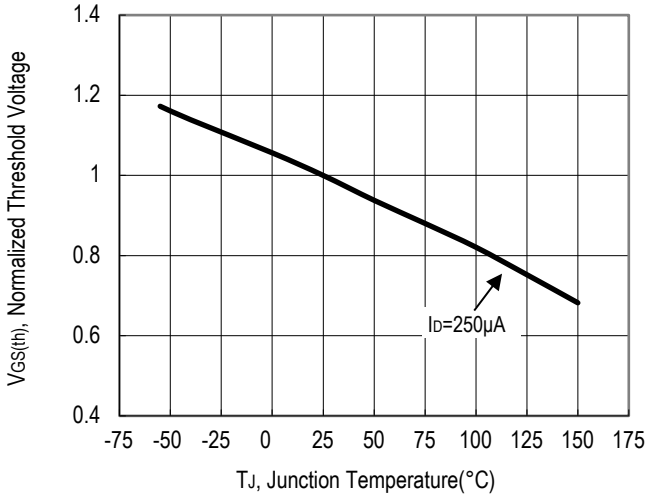
THERMAL CHARACTERISTICS

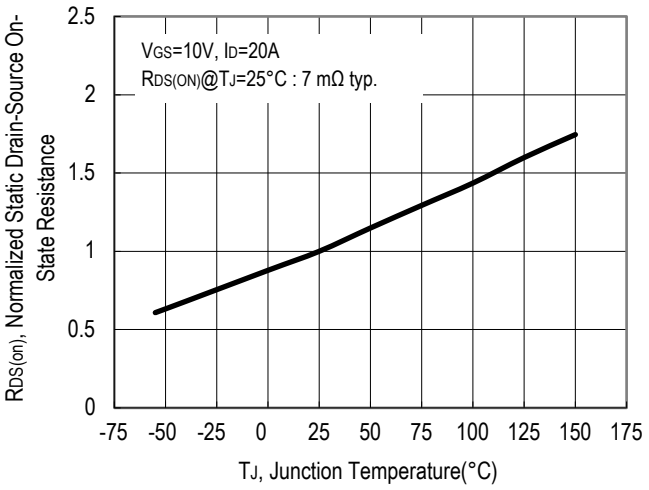
THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	RθJc		4	℃ /W
Junction-to-Ambient	RθJA		60	℃ /W

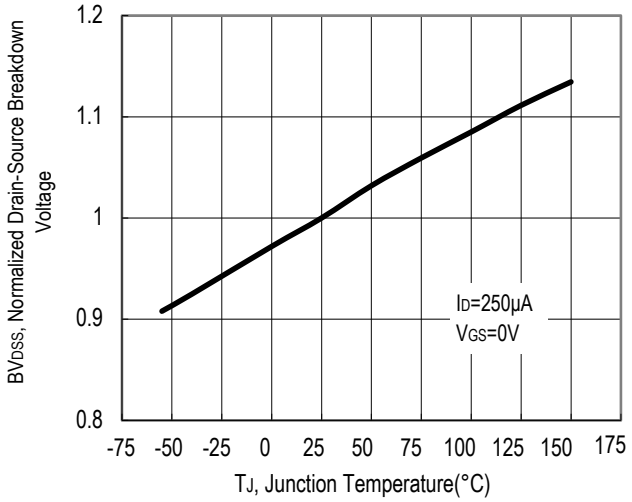
PARAMETER	SYNBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltege Gate	V(BR)DSS	VGS=0V,ID=250μA	30			V
Threshold Voltage	VGS(th)	VDS=VGS,ID=250μA	1	1.6	2.5	
Gate-Body Leakage	IGSS	VDS=0V,VGS=± 2 0V			±100	nA
Zero Gate Voltage Dain Current	IDSS	VDS=48V,VGS=0 V			1	μA
		VDS=20V,VGS=0V,TJ=125 ℃			30	
Drain-Source On- State Resistance1	RDS(ON)	VGS=4.5V,ID=15A		11	16	mΩ
		VGS=10V,ID=20A		7	12	
Forward Trans conductance[1]	gfs	VDS=5V,ID=16A		15		S
DYNAMIC						
Input Capacitance Output	Ciss	VGS=0V,VDS=15V,f=1MHZ		1480		pF
Capacitance	Coss			276		
Reverse Transfer Capacitance Gate	Crss			31		
Resistance	RG	VGS=0V,f=1MHZ		3.5		Ω
Total Gate Charge[2]	Qg(vgs=10V)	VDS=30V (BR)DSS, ID = 20A		15.5		nC
	Qg(vgs=4.5V)			12.8		
Gate Source Charge[2]	QgS(VGS=10V)			8.5		
	QgS(VGS=4.5V)			6.7		
Gate-Drain Charge[2]	Qgd(VGS=10V)			4.7		
	Qgd(VGS=4.5V)			3.2		
Tum-On Delay Time[2]	td(on)	VDS=30V,RL=1.5Ω ID=20A,VGS=10V.RGS=6Ω		1.6		nS
Rise Time[2]	t r			17		
Tum-Off Delay Time[2]	td(off)			33		
Fall Time[2]	t r			10.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS(TJ=25℃)						
Continuous Current	IS			24		A
Forward Voltage[1]	VSD	IF=IS,VGS=0V		0.75	1.1	V
Reverse Recovery Time	Trr	IF=20V,d1f/dt=100A/μs		24		nS
Reverse Recovery Charge	Qrr			16		nC

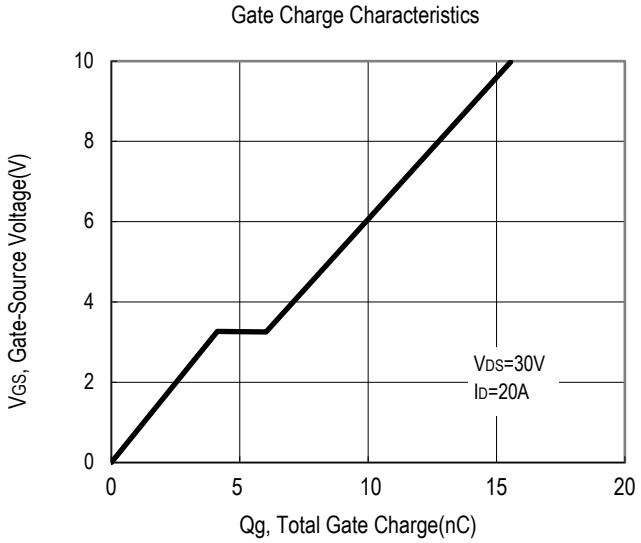
Note
b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .
c. Independent of operating production testing .

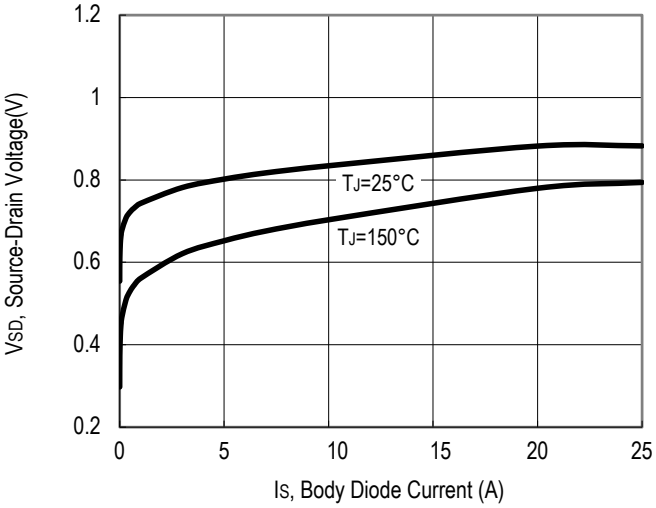

80
60
40
20
0
0
1
2
3
4
5
4.5V
10V,9V,8V,7V,6V,5V
4V
3.5V
VGS=3V
ID, Drain Current (A)
VDS, Drain-Source Voltage(V)

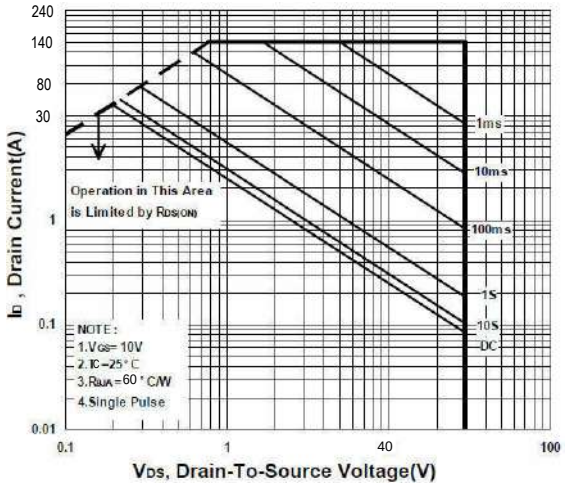

1.4
1.2
1
0.8
0.6
0.4
-75 -50 -25 0 25 50 75 100 125 150 175
ID=250μA
VGS(th), Normalized Threshold Voltage
TJ, Junction Temperature(°C)


2.5
2
1.5
1
0.5
0
-75 -50 -25 0 25 50 75 100 125 150 175
VGS=10V, ID=20A
RDS(ON)@TJ=25°C : 7 mΩ typ.
RDS(on), Normalized Static Drain-Source On-State Resistance
TJ, Junction Temperature(°C)

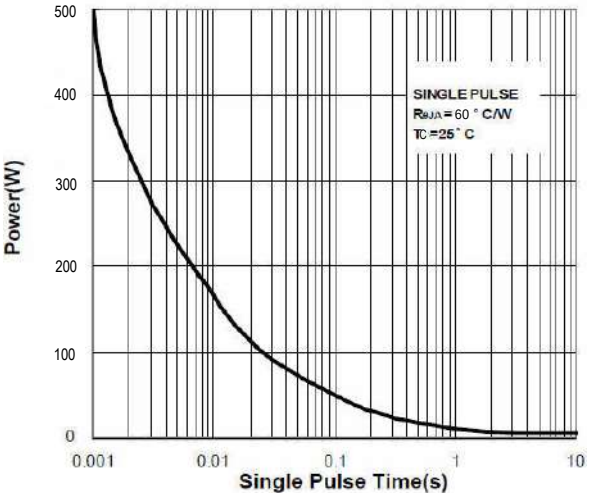

1.2
1.1
1
0.9
0.8
-75 -50 -25 0 25 50 75 100 125 150 175
ID=250μA
VGS=0V
BVDSS, Normalized Drain-Source Breakdown Voltage
TJ, Junction Temperature(°C)


Gate Charge Characteristics
10
8
6
4
2
0
0
5
10
15
20
VDS=30V
ID=20A
VGS, Gate-Source Voltage(V)
Qg, Total Gate Charge(nC)


1.2
1
0.8
0.6
0.4
0.2
0
5
10
15
20
25
TJ=25°C
TJ=150°C
VSD, Source-Drain Voltage(V)
IS, Body Diode Current (A)



Safe Operating Area



Single Pulse Maximum Power Dissipation

Transient Thermal Response Curves