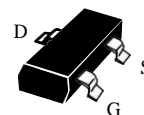# N-Channel High Density Trench MOSFET

Features:
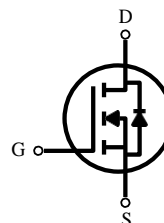
● Super high dense cell trench design for low $R_{DS(on)}$.

● Rugged and reliable.

● Surface Mount package.

SOT-23-3L

PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m-ohm) Max
100V	2	120 @ V_{GS} = 10V
	1	150 @ V_{GS} = 4.5V

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous[a] @ T_A = 25 °C		I_D	4.1	A
-Pulse[b]		I_{DM}	16.4	A
Drain-Source Diode Forward Current [a]		I_S	1.2	A
Maximum Power Dissipation [a]	T_A=25°C	P_D	1	W
	T_A=75°C		0.65	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	- 55 to 150	°C

THERMAL CHARACTERISTICS

	Symbol		Unit
Thermal Resistance,Junction-to-Ambient [a]	R_{thJA}	125	°C/W

Note
a. Surface Mounted on FR4 Board , t ≤ 10sec .
b. Pulse width limited by maximum junction temperature.

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V$, $I_D = 250uA$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V$, $V_{GS} = 0V$			1	uA
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm20V$, $V_{DS} = 0V$			±100	uA
ON CHARACTERISTICS [b]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250uA$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 2A$		92	120	m-ohm
		$V_{GS} = 4.5V$, $I_D = 1A$		120	150	
Forward Transconductance	g_{fs}	$V_{DS} = 10V$, $I_D = 2A$		11		S
DRAIN-SOURCE DIODE CHARACTERISTICS [b]						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V$, $I_S = 1.2A$			1.2	V
DYNAMIC CHARACTERISTICS [c]						
Input Capacitance	C_{ISS}	$V_{DS} = 50V$, $V_{GS} = 0V$ f = 1.0MHz		185		pF
Output Capacitance	C_{OSS}			31		pF
Reverse Transfer Capacitance	C_{RSS}			2.8		pF
SWITCHING CHARACTERISTICS [c]						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 50V$, $I_D = 1A$ $V_{GEN} = 10V$ $R_L = 3$ ohm $R_{GEN} = 3ohm$		4.8		ns
Rise Time	t_r			19		ns
Turn-Off Delay Time	$t_{D(OFF)}$			17		ns
Fall Time	t_f			6.2		ns
Total Gate Charge	Q_g	$V_{DS} = 50V$ $I_D = 2A$ $V_{GS} = 10V$		3.6		nC
Gate-Source Charge	Q_{gs}			0.68		nC
Gate-Drain Charge	Q_{gd}			0.9		nC

Note

b. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2% .

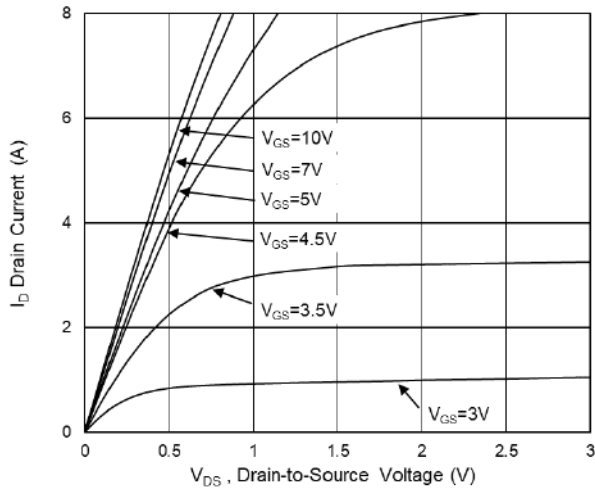c. Guaranteed by design , not subject to production testing .
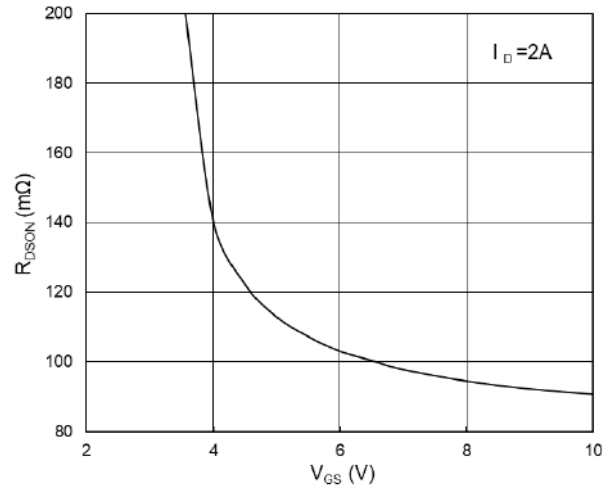
Fig.1 Typical Output Characteristics
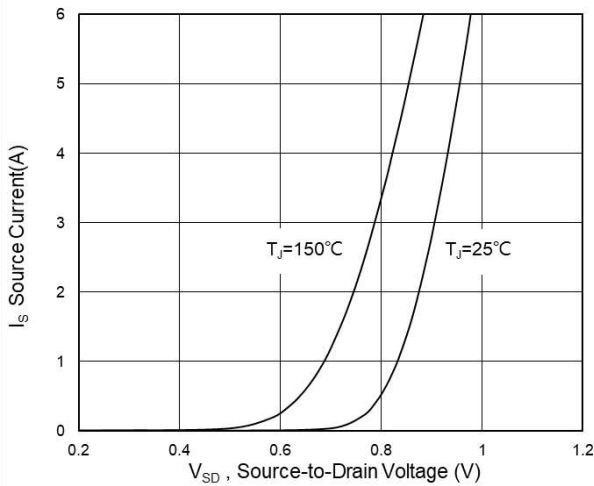
Fig.2 On-Resistance vs G-S Voltage

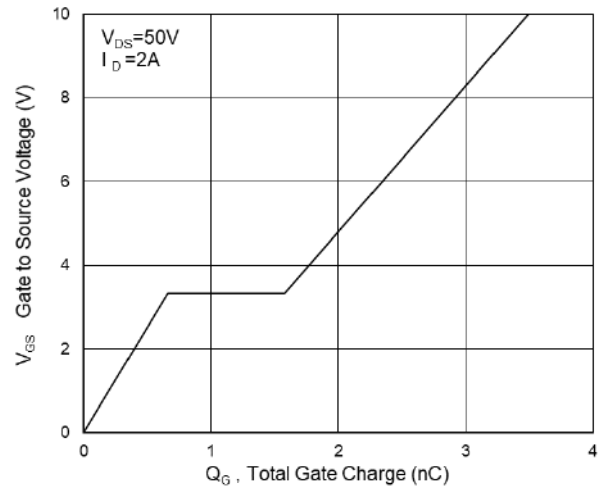**Fig.3 Source Drain Forward Characteristics**
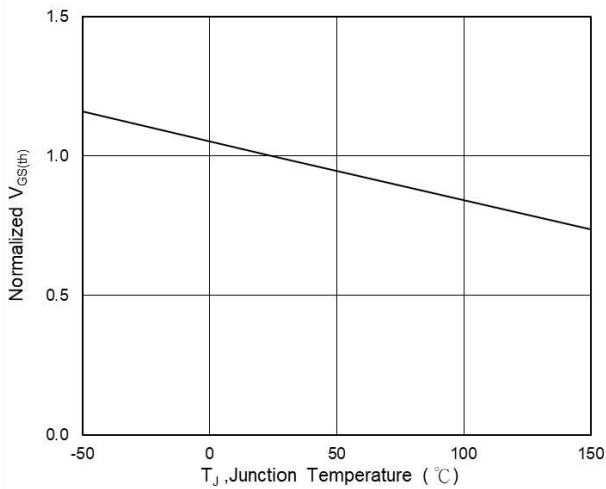
Fig.4 Gate-Charge Characteristics

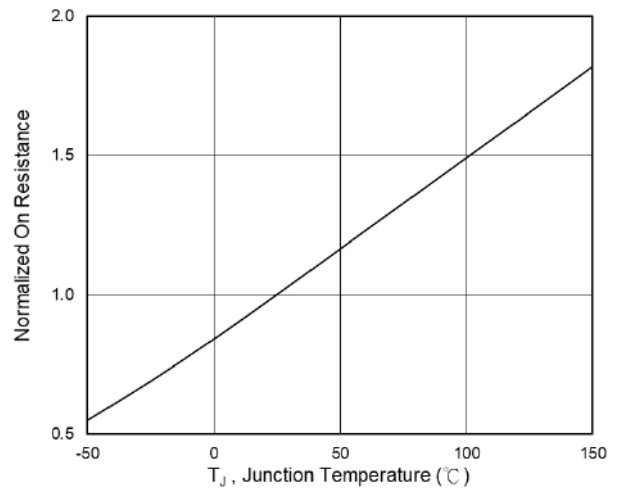**Fig.5 Normalized $V_{GS(th)}$ vs T_J**

Fig.6 Normalized R_{DSON} vs T_J

Fig.7 Capacitance

Fig.8 Safe Operating Area

$$D = T_{ON}/T$$
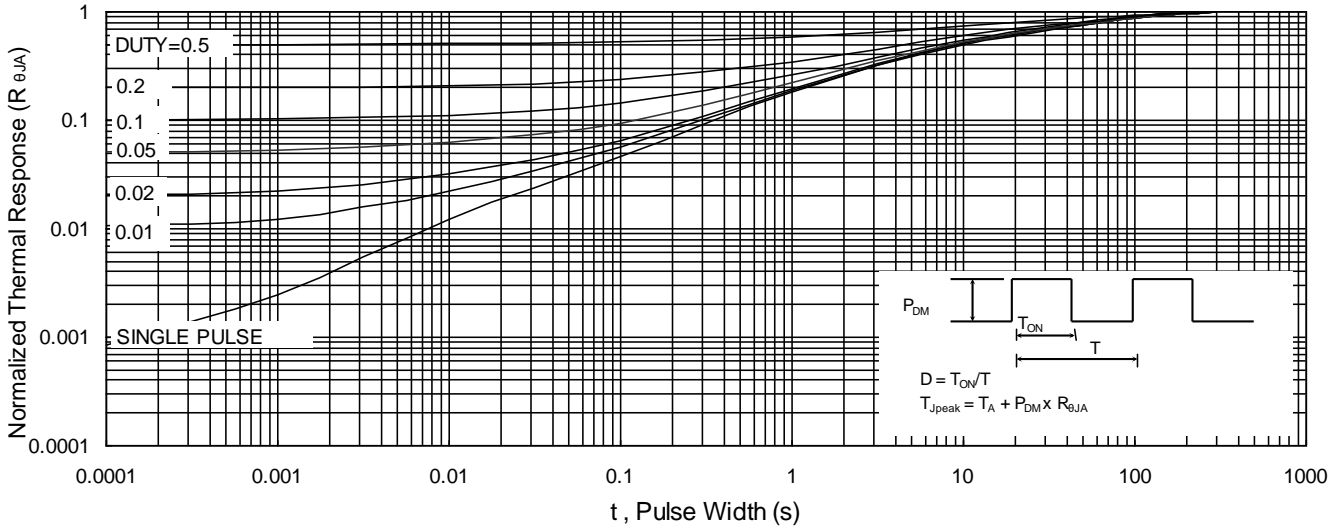$$T_{Jpeak} = T_A + P_{DM} \times R_{\theta JA}$$

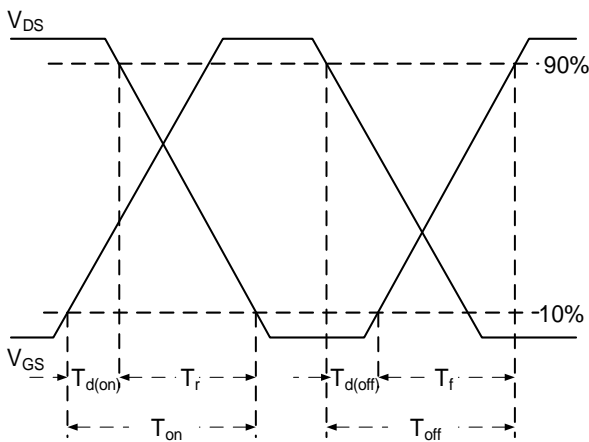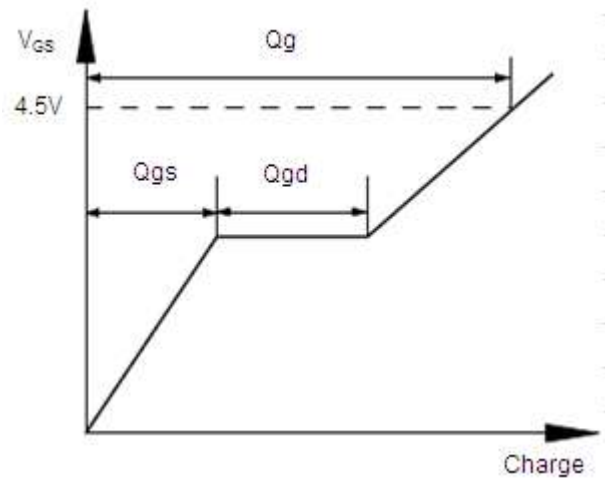**Fig.9 Normalized Maximum Transient Thermal Impedance**

Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform