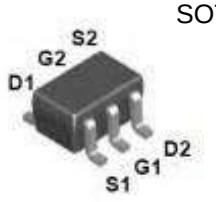
Dual N-Channel High Density Trench MOSFET

Features:

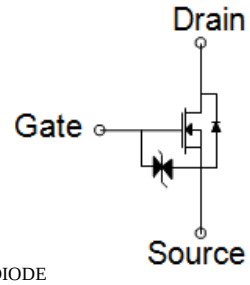
- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

SOT-363



PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m-ohm) Max
20V	0.6A	500 @ V_{GS} = 4.5V
	0.4A	800 @ V_{GS} = 2.5V



ESD PROTECTION DIODE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 ℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Drain Current-Continuous[a] @ T_A = 25 ℃		I_D	0.8	A
-Pulse[b]		I_{DM}	3.2	A
Drain-Source Diode Forward Current[a]		I_S	0.6	A
Maximum Power Dissipation[a]	T_A=25℃	P_D	0.5	W
	T_A=75℃		0.3	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	- 55 to 150	℃

THERMAL CHARACTERISTICS

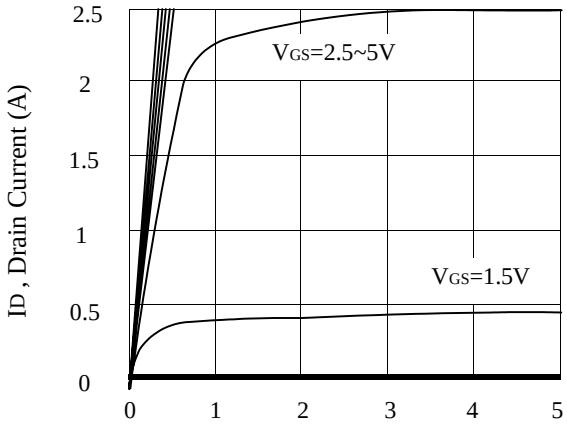
Thermal Resistance,Junction-to-Ambient[a]	R_{thJA}	250	℃/W

Note
a. Surface Mounted on FR4 Board , t ≤ 10sec.
b. Pulse width limited by maximum junction temperature.

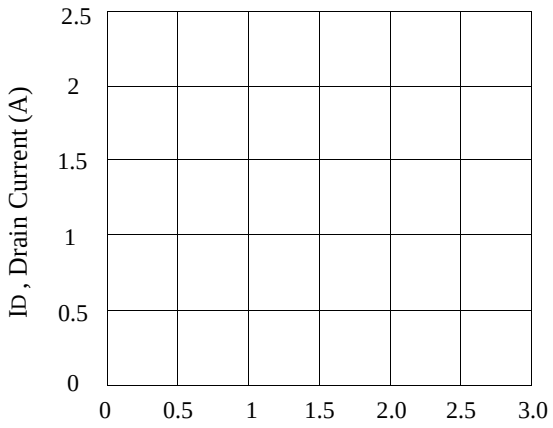
ELECTRICAL CHARACTERISTICS (T_A = 25 ℃ unless otherwisenoted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V , I_D = 250uA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V , V_{GS} = 0V			1	uA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±8V , V_{DS} = 0V			±10	uA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250uA	0.5	0.7	1	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5V , I_D = 0.6A		300	500	m-ohm
		V_{GS} = 2.5V , I_D = 0.4A		600	800	
Forward Transconductance	g_{fs}	V_{DS} = 5V , I_D = 0.3A		3		S
DRAIN-SOURCE DIODE CHARACTERISTICS[b]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V , I_S = 0.3A		0.7	1.2	V
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} = 6V , V_{GS} = 0V f = 1.0MHz		42		pF
Output Capacitance	C_{OSS}			23		pF
Reverse Transfer Capacitance	C_{RSS}			19		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 6V , I_D = 0.3A V_{GEN} = 4.5V R_L = 6 ohm R_{GEN} = 6 ohm		5	9	ns
Rise Time	t_r			15	42	ns
Turn-Off Delay Time	$t_{D(OFF)}$			25	28	ns
Fall Time	t_f			7.6		ns
Total Gate Charge	Q_g	V_{DS} = 6V I_D = 0.3A V_{GS} = 4.5V		3.4		nC
Gate-Source Charge	Q_{gs}			2.5		nC
Gate-Drain Charge	Q_{gd}			1.7		nC

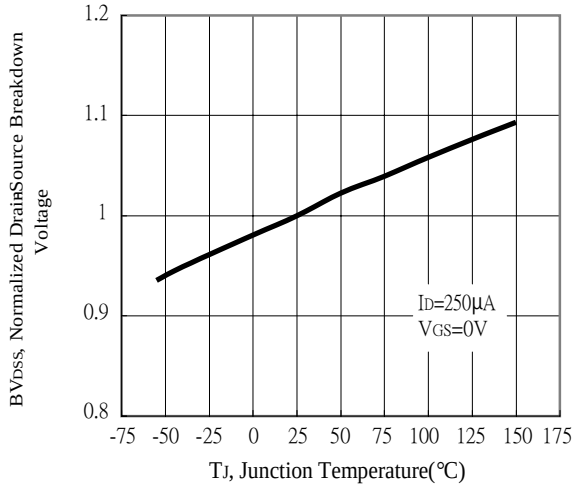
Note
b. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2%.
c. Guaranteed by design , not subject to production testing.

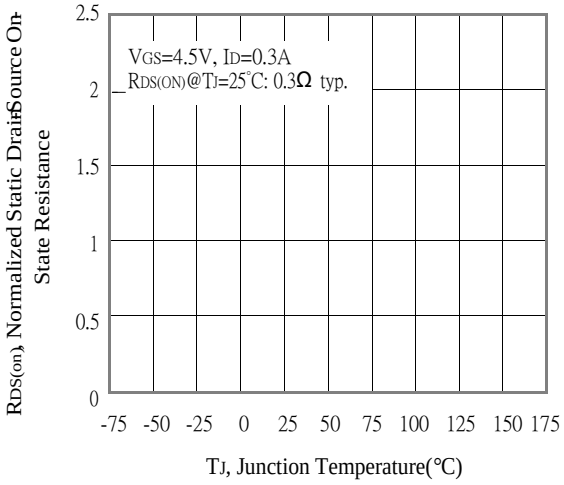


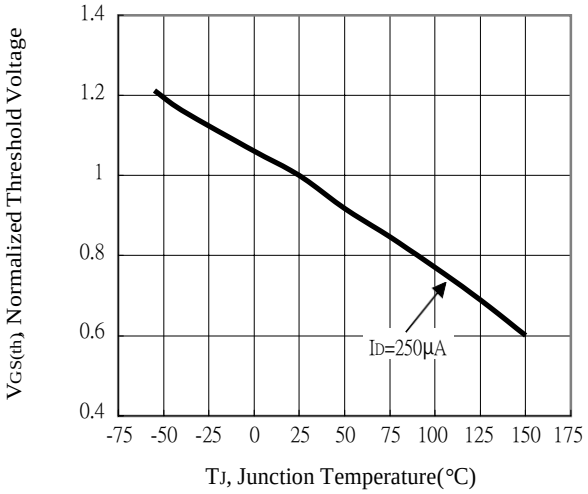
Output Characteristics

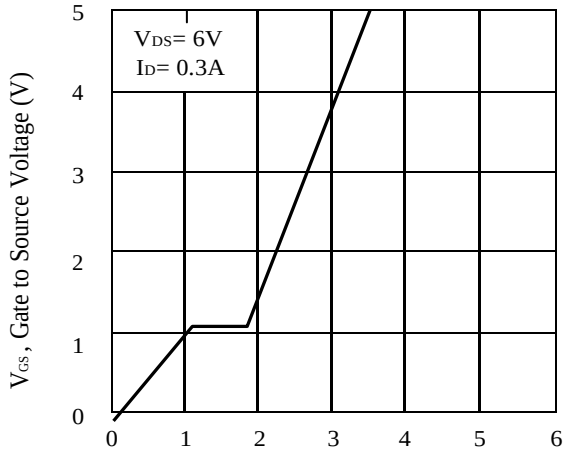


Transfer Characteristics

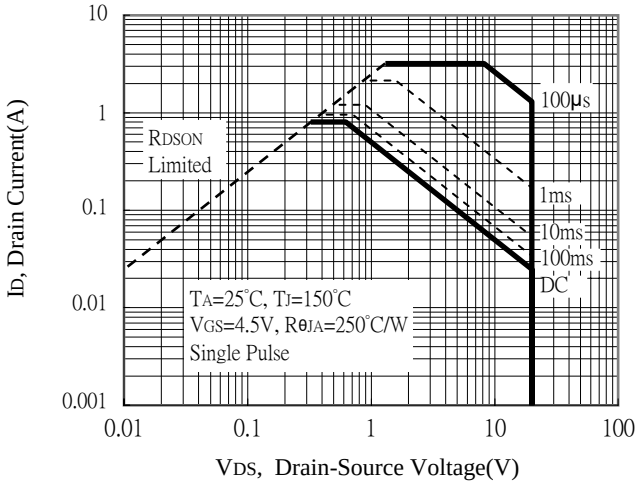




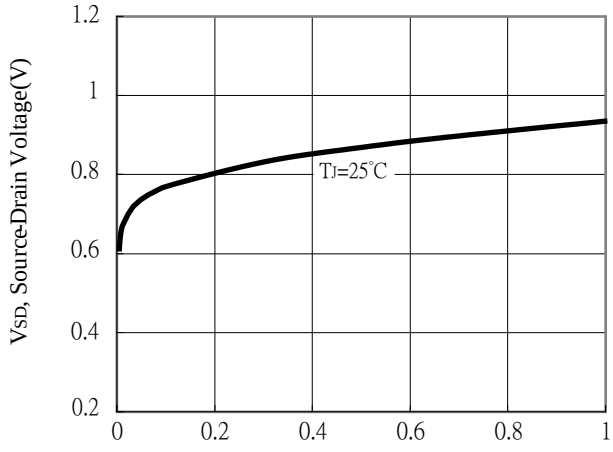




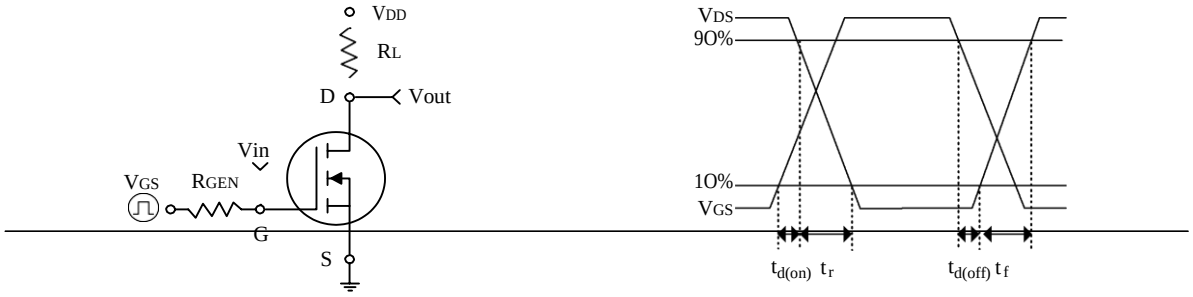
Gate Charge



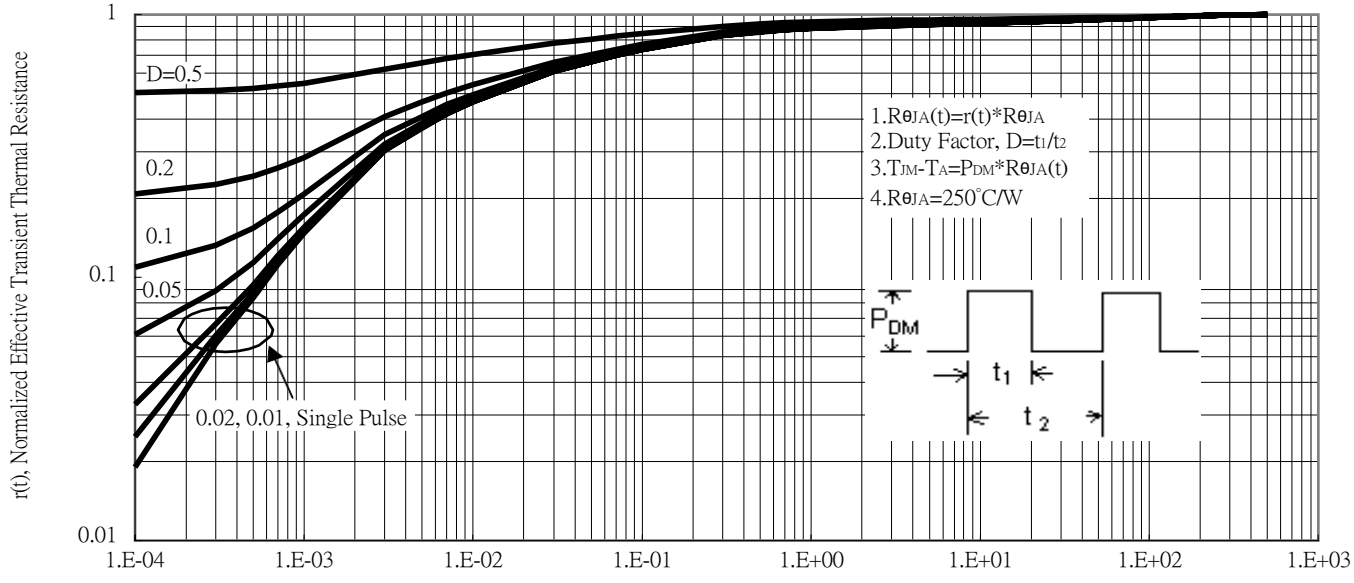
Maximum Safe Operating Area



Body Diode Forward Voltage Variation with Source Current



Switching Test Circuit and Switching Waveforms



Normalized Thermal Transient Impedance Curve