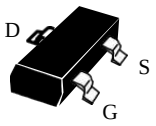
P-Channel High Density Trench MOSFET

Features:

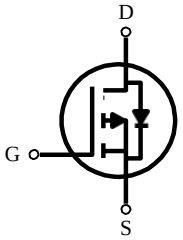
- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- SOT-23-3L package.

SOT-23-3L



PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (mΩ) Max
-30V	-6 A	32 @ V_{GS} = -10V
		58 @ V_{GS} = -4.5V
		78 @ V_{GS} = -2.5V



DEVICE MARKING

KW2605GE= 2605

ABSOLUTE MAXIMUM RATINGS (T_A = 25 ℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous[a] @ T_A = 25 ℃	I_D	-6	A
-Pulse[b]	I_{DM}	-24	A
Drain-Source Diode Forward Current[a]	I_S	-2.3	A
Maximum Power Dissipation[a]	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	- 55 to 150	℃

THERMAL CHARACTERISTICS

Parameter	Symbol	Typ[c]	Max	Unit
Thermal Resistance,Junction-to-Ambient[a]	R_{thJA}	75	100	℃/W

Note：
a. Surface Mounted on FR4 Board , t ≤ 5sec .
b. Pulse Test：Pulse width ≤ 300us , Duty Cycle ≤ 2% .

ELECTRICAL CHARACTERISTICS (T_A = 25 ℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V , I_D = -250uA	- 30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V , V_{GS} = 0V			-1	uA
Gate-Body Leakage	I_{GSS}	V_{GS} = -12V , V_{DS} = 0V			-100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = -250uA	-1	-1.5	-2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10V , I_D = -4.2A		25	32	mΩ
		V_{GS} = -4.5V , I_D = -4.0A		43	58	mΩ
		V_{GS} = -2.5V , I_D = -1.0A		65	78	mΩ
DRAIN-SOURCE DIODE CHARACTERISTICS[b]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V , I_S = -1.0A			-1.0	V
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} = 15V , V_{GS} = 0V f = 1.0MHz		987		pF
Output Capacitance	C_{OSS}			246		pF
Reverse Transfer Capacitance	C_{RSS}			110		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = -15V , I_D = -1A V_{GEN} = -4.5V R_L = 15 Ω R_{GEN} = 10 Ω		38		ns
Rise Time	t_r			4.2		ns
Turn-Off Delay Time	$t_{D(OFF)}$			13		ns
Fall Time	t_f			7.8		ns
Total Gate Charge	Q_g	V_{DS} = -15V I_D = -1A V_{GS} = -10V		18.2		nC
Gate-Source Charge	Q_{gs}			4.2		nC
Gate-Drain Charge	Q_{gd}			5.1		nC

Note
b. Pulse Test：Pulse width ≤ 300us , Duty Cycle ≤ 2% .
c. Guaranteed by design , not subject to production testing.

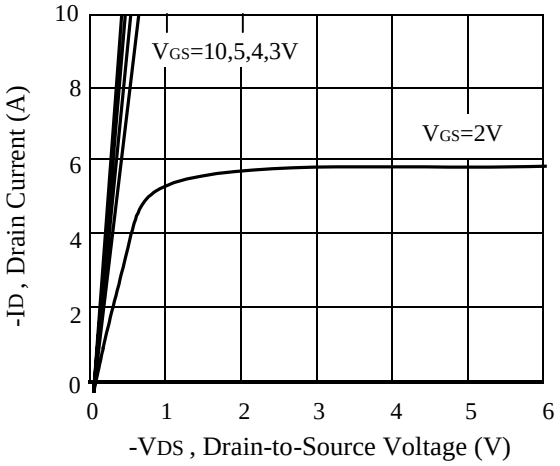


Figure 1. Output Characteristics

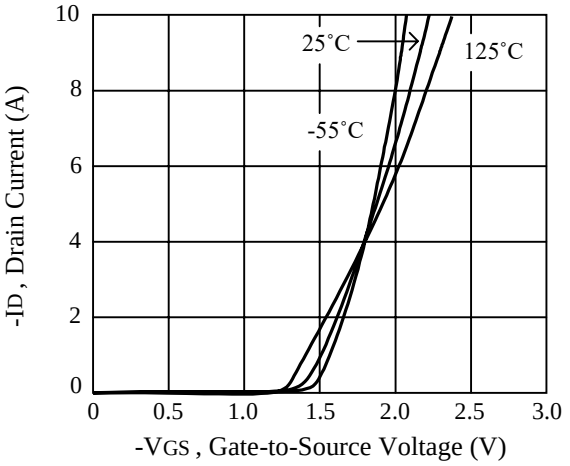


Figure 2. Transfer Characteristics

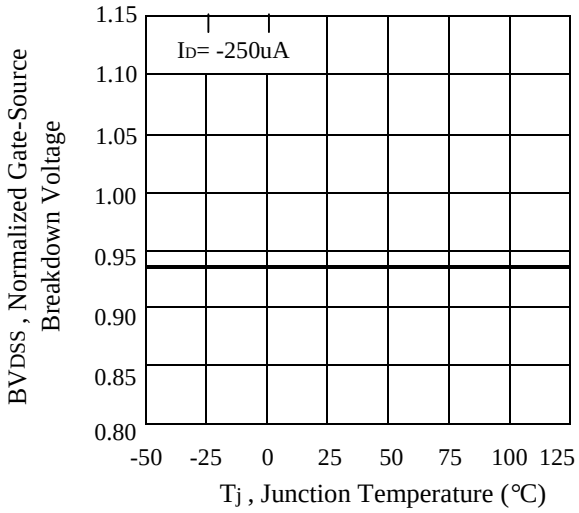


Figure 6. Breakdown Voltage Variation with Temperature

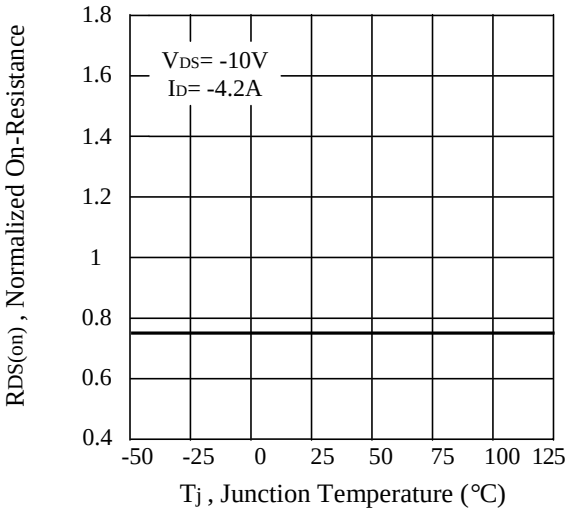


Figure 4. On-Resistance Variation with Temperature

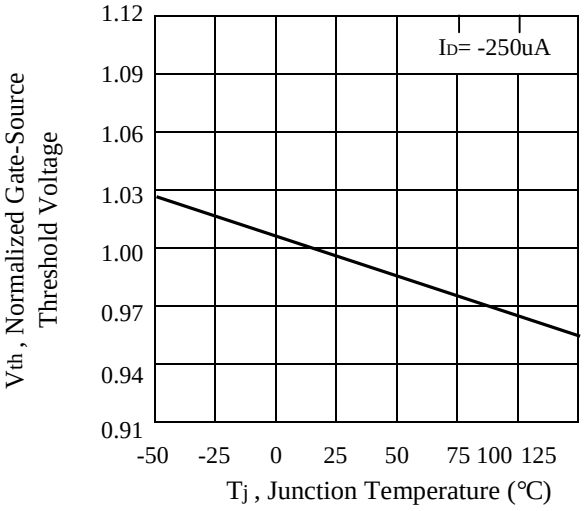


Figure 5. Gate Threshold Variation with Temperature

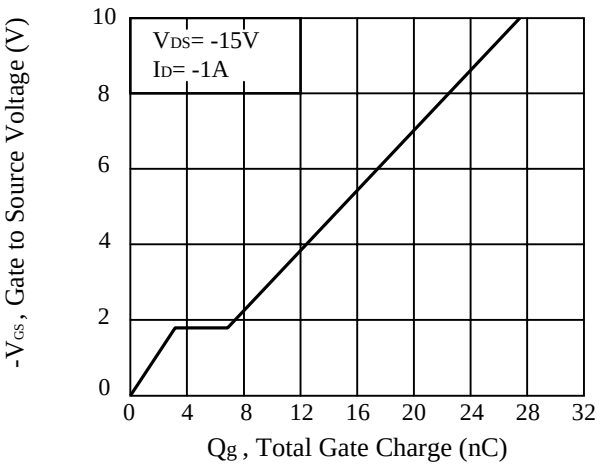


Figure 7. Gate Charge

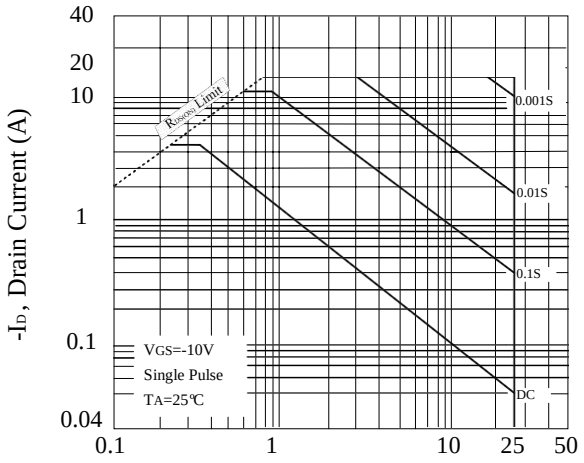


Figure 9. Maximum Safe Operating Area

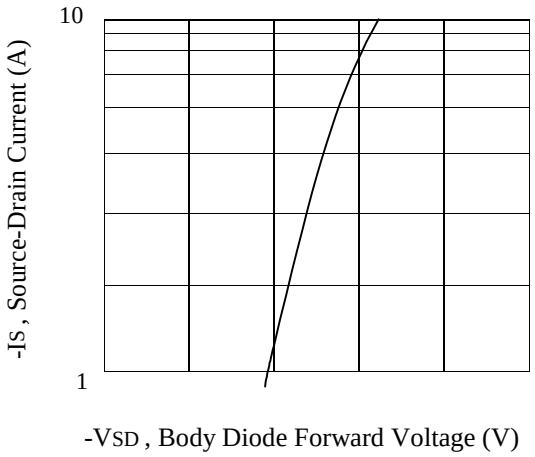
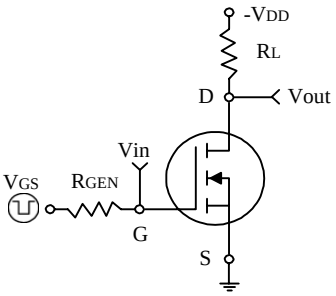


Figure 8. Body Diode Forward Voltage Variation with Source Current



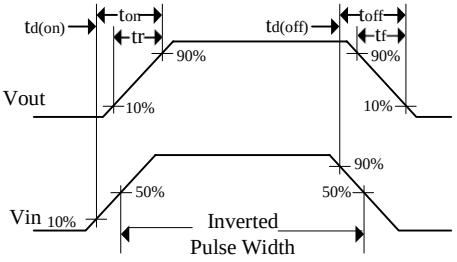


Figure 10. Switching Test Circuit and Switching Waveforms

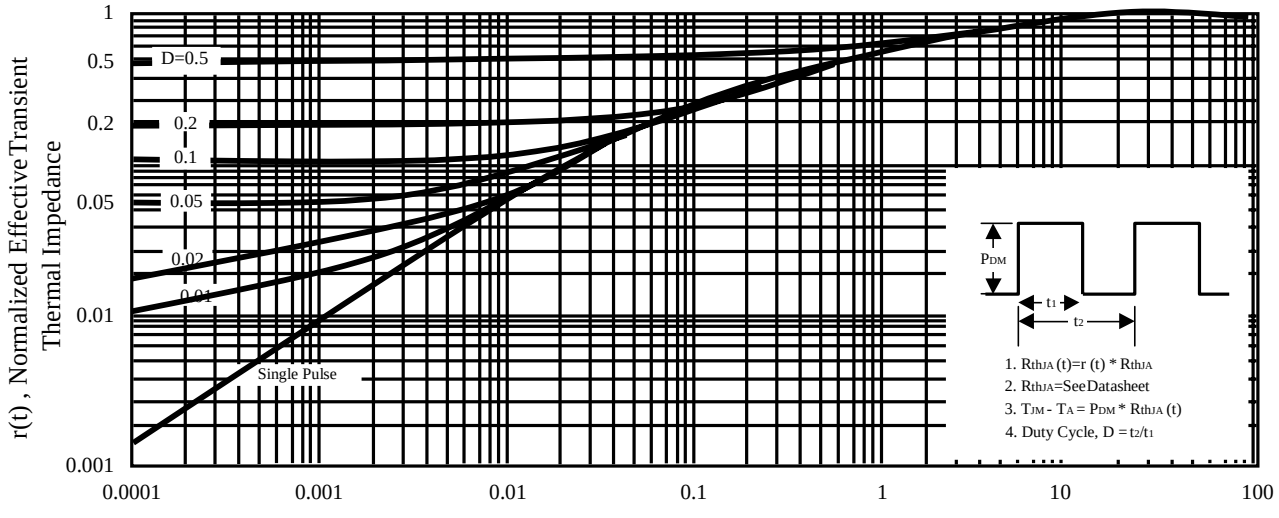
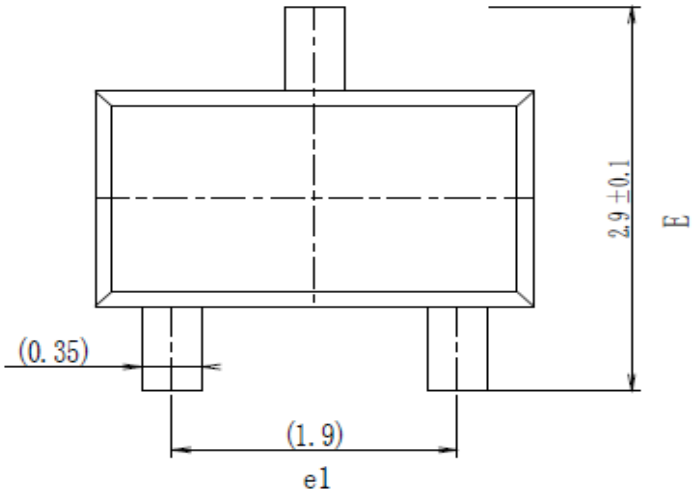
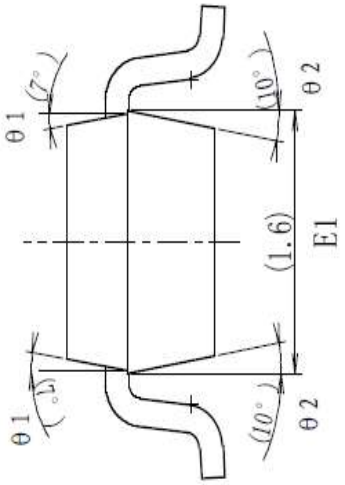
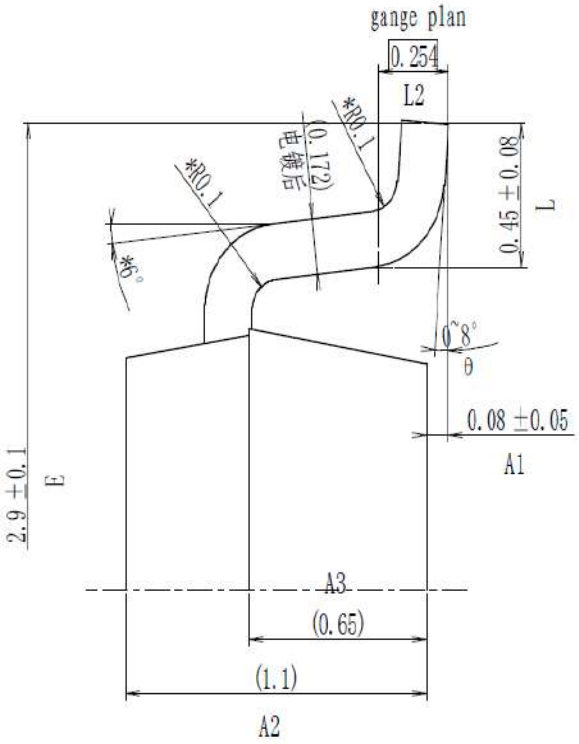
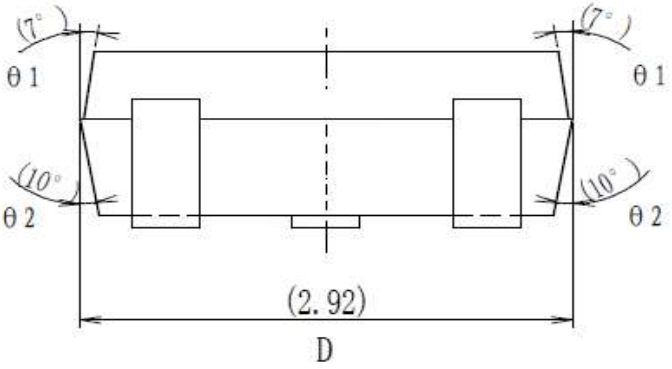


Figure 11. Normalized Thermal Transient Impedance Curve









NOTE:
1. ALL DIMENSION ARE METRIC.
2. PACKAGE SURFACE TO BE MATTE FINISH : Ra 0.3 μM MAX.
3. MAX MISMATCH OF TOP AND BTM PACKAGE TO BE 0.038mm.
4. MAX OFFSET/MISALIGNMENT OF PACKAGE TO L/F TO BE 0.05.
5. LEAD FRAM MATERIAL : A194 F.H THICKNESS : 0.152±0.008.