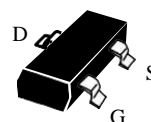


N-Channel High Density Trench MOSFET

Features:

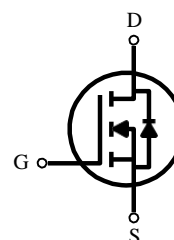
- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

SOT-23-3L



PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m-ohm) Max
20V	8A	13@ $V_{GS} = 4.5V$
	6A	15@ $V_{GS} = 2.5V$



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous ^a @ $T_A = 25\text{ }^\circ\text{C}$ -Pulse ^b	I_D	12	A
	I_{DM}	48	A
Drain-Source Diode Forward Current ^a	I_S	4	A
Maximum Power Dissipation ^a	P_D	$T_A=25\text{ }^\circ\text{C}$	1.25
		$T_A=75\text{ }^\circ\text{C}$	0.75
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$
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Note
a. Surface Mounted on FR4 Board , $t \leq 10\text{sec}$.
b. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V , I _D = 250uA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V , V _{GS} = 0V			1	uA
Gate-Body Leakage	I _{GSS}	V _{GS} = 12V , V _{DS} = 0V			100	nA
ON CHARACTERISTICS^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	0.5	0.7	1	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 4.5V , I _D = 8A		10	13	m-ohm
		V _{GS} = 2.5V , I _D = 6A		12	15	
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V , I _s = 1.7A		0.8	1.3	V
DYNAMIC CHARACTERISTICS^c						
Input Capacitance	C _{ISS}	V _{DS} = 8V , V _{GS} = 0V f = 1.0MHz		628		pF
Output Capacitance	C _{OSS}			212		pF
Reverse Transfer Capacitance	C _{RSS}			158		pF
SWITCHING CHARACTERISTICS^c						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 10V , I _D = 3A V _{GEN} = 4.5V R _L = 3.3 ohm R _{GEN} = 6 ohm		8.7		ns
Rise Time	t _r			4.2		ns
Turn-Off Delay Time	t _{D(OFF)}			18		ns
Fall Time	t _f			6.1		ns
Total Gate Charge	Q _g	V _{DS} = 10V , I _D = 3A V _{GS} = 4.5V		6.2		nC
Gate-Source Charge	Q _{gs}			3.3		nC
Gate-Drain Charge	Q _{gd}			1.9		nC

Note

b. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2% .

c. Guaranteed by design , not subject to production testing .

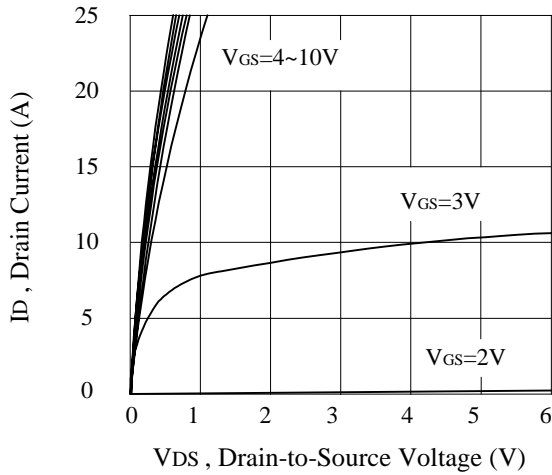


Figure 1. Output Characteristics

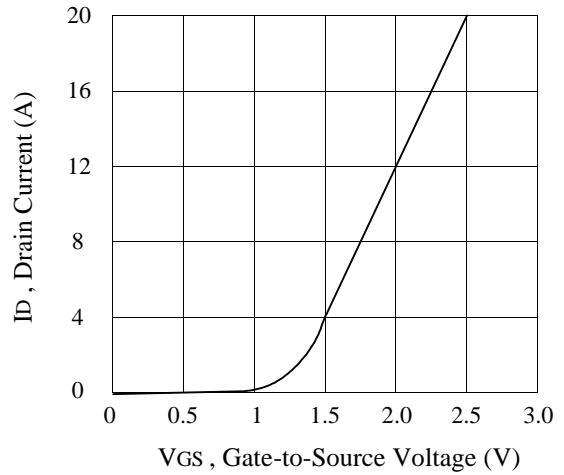


Figure 2. Transfer Characteristics

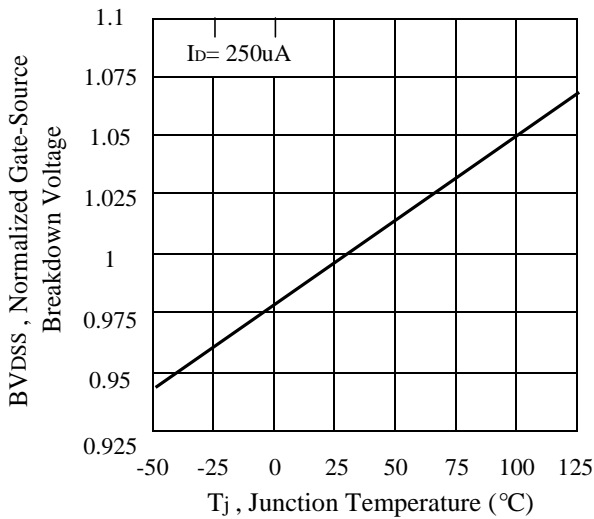


Figure 3. Breakdown Voltage Variation with Temperature

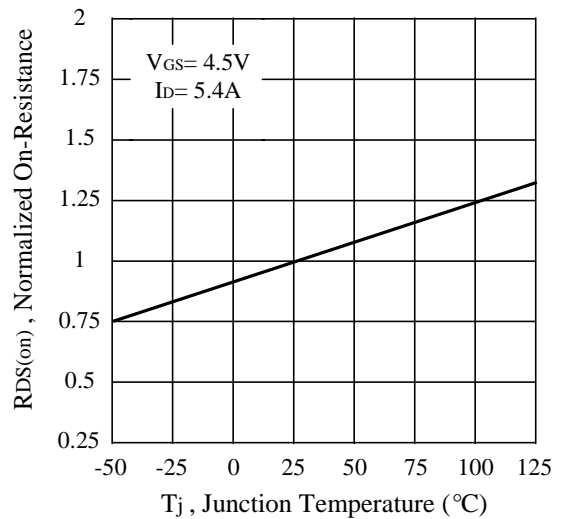


Figure 4. On-Resistance Variation with Temperature

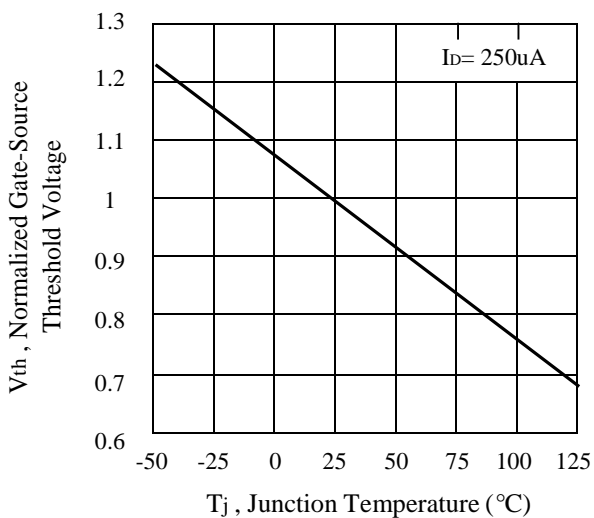


Figure 5. Gate Threshold Variation with Temperature

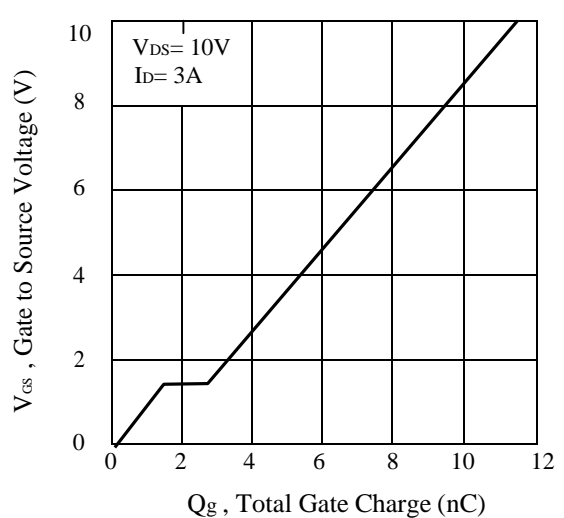


Figure 6. Gate Charge

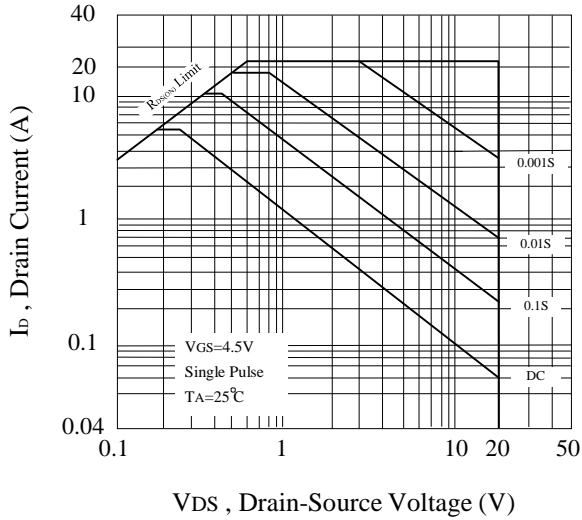


Figure 7. Maximum Safe Operating Area

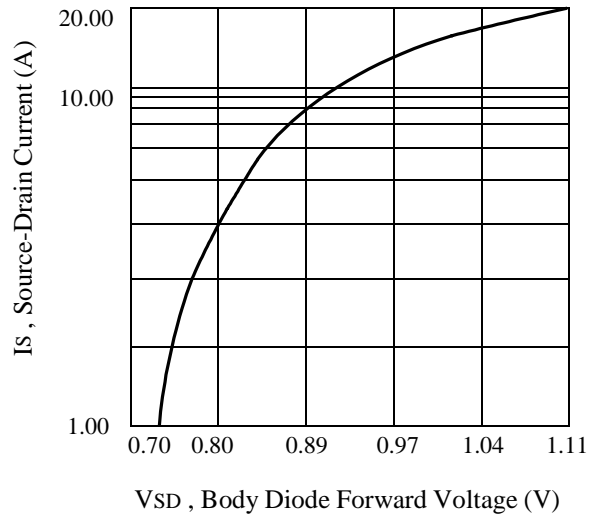


Figure 8. Body Diode Forward Voltage Variation with Source Current

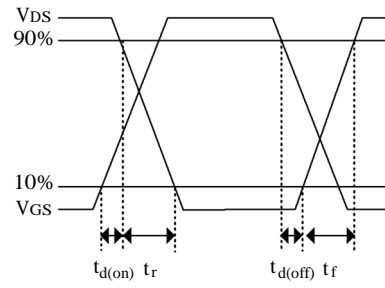
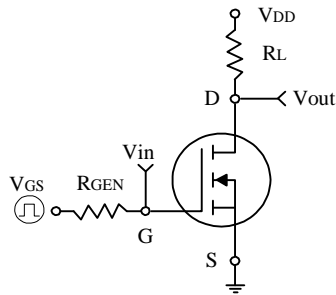


Figure 9. Switching Test Circuit and Switching Waveforms

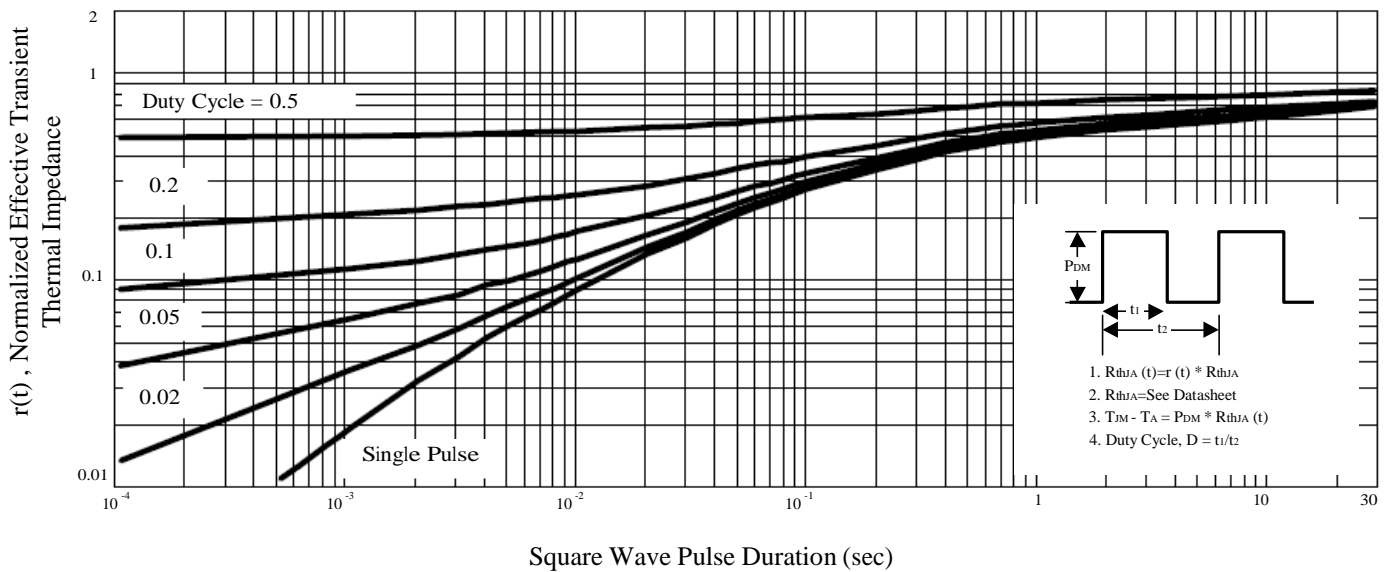
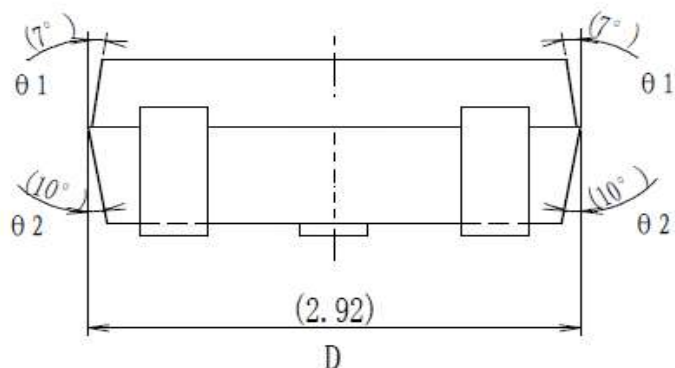
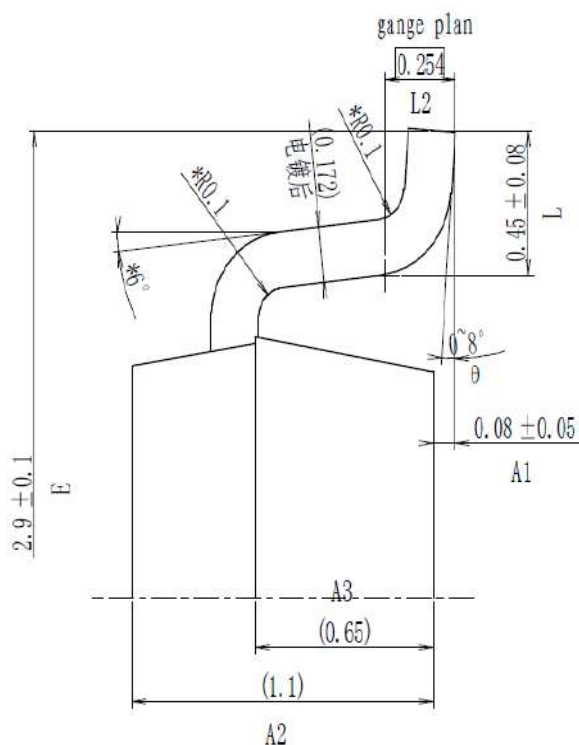
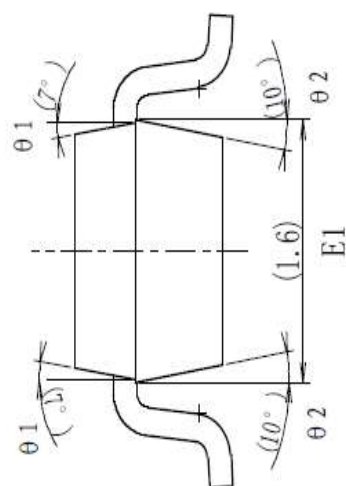
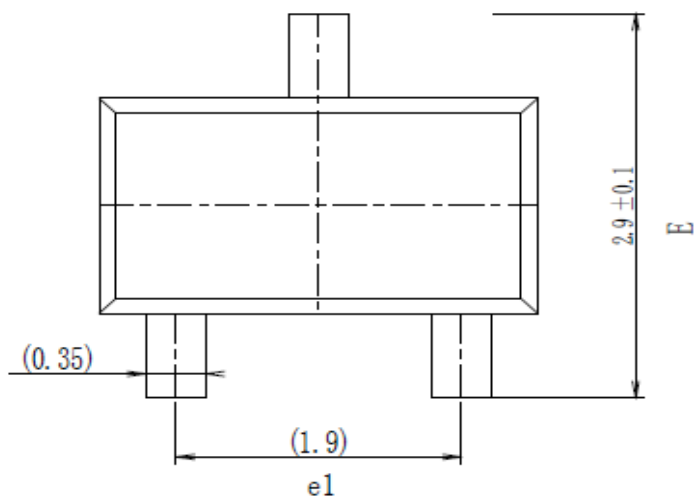


Figure 10. Normalized Thermal Transient Impedance Curve



NOTE:

1. ALL DIMENSION ARE METRIC.
2. PACKAGE SURFACE TO BE MATTE FINISH ; R_a 0.3 μm MAX.
3. MAX MISMATCH OF TOP AND BTM PACKAGE TO BE 0.038mm.
4. MAX OFFSET/MISALIGNMENT OF PACKAGE TO L/F TO BE 0.05.
5. LEAD FRAM MATERIAL ; A194 F.H THICKNESS ; 0.152 ± 0.008 .