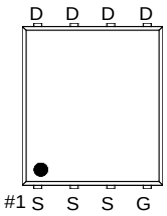
P -Channel High Density Trench MOSFET

FEATURES

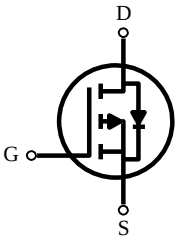
- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

PDFN3333



G. GATE
D. DRAIN
S. SOURCE

PRODUCT SUMMARY		
$V_{(BR)DSS}$	$R_{DS(on)}$ (mΩ) Max	I_D
-40V	13 @ V_{GS} = -10V	-40A
	19 @ V_{GS} = -4.5V	



ABSOLUTE MAXIMUM RATINGS (TA = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	TC=25℃	I_D	-40	A
	TC=100℃		-25	
Pulsed Drain Current (Note 1)		I_{DM}	-120	
Avalanche Current		I_{AS}	-54	
Single Pulse Avalanche Energy	L = 0.1mH	E_{AS}	146	mJ
Maximum Power Dissipation (Note 1)	TC=25ºC	P_D	-54	W
	TC=100ºC		19.8	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	- 55 to 150	°C

TYPICAL THERMAL CHARACTERISTICS (Note 1)

Thermal Resistance,Junction-to-Case	R_{thJC}	4	°C/W
Thermal Resistance Junction-Ambient	R_{thJA}	62	°C/W

Note：

1. Pule width limited by maximum junction temperature.

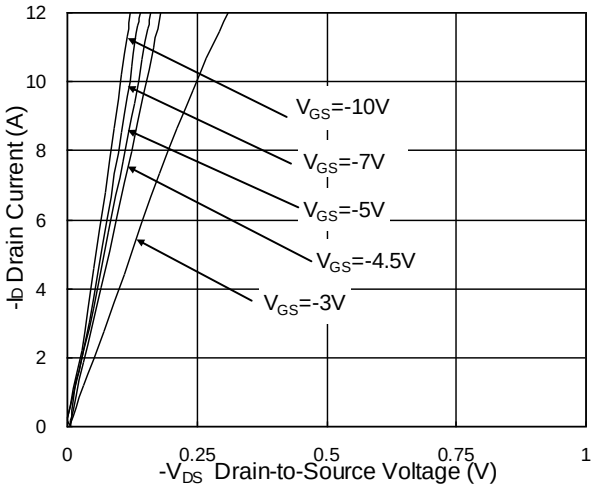
ELECTRICAL CHARACTERISTICS (TA = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V , I_D = -250uA	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -32V , V_{GS} = 0V, Tj = 25℃			-1	uA
		V_{DS} = -32V , V_{GS} = 0V , Tj = 100℃			-10	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V , V_{DS} = 0V			±100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = VGS , I_D = 250uA	-1	-1.6	-2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10V , I_D = -20A		11	13	mΩ
		V_{GS} = -4.5V , I_D = -12A		15.5	19	mΩ
Forward Transconductance	gfs	V_{DS} = -5V , I_D= -10A		23		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = -15V , V_{GS} = 0V f = 1.0MHz		3480		pF
Output Capacitance	C_{OSS}			321		pF
Reverse Transfer Capacitance	C_{RSS}			217		pF
Gate Resisance	Rg	V_{DS} = 0V , V_{GS} = 0V , f = 1.0MHz		7		Ω
SWITCHING CHARACTERISTICS (Note 3)						
Turn-On Delay Time	$td_{(ON)}$	V_{DD} = -15V , I_D = -6A , V_{GS} = -10V R_{GS}= 3.3Ω		40		nS
Rise Time	tr			35.2		nS
Turn-Off Delay Time	$td_{(OFF)}$			100		nS
Fall Time	tf			9.6		nS
Total Gate Charge (10V)	Qg	V_{DS} = -20V, I_D = -12A V_{GS} = -4.5V		44		nC
Total Gate Charge (4.5V)	Qg			28		nC
Gate-Source Charge	Qgs			7.7		nC
Gate-Drain Charge	Qgd			7.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Continuous Current	I_S			-40		A
Diode Forward Voltage (Note 2)	V_{SD}	V_{GS} = 0V , I_S = I_F		-0.7	-1.1	V

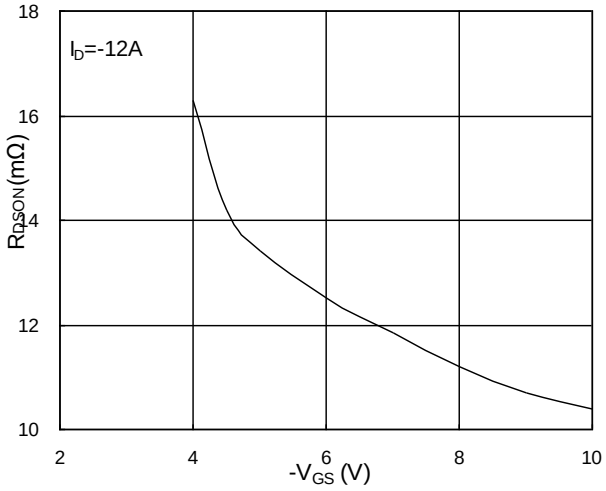
Note：

2. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2%
3. Independent of operating production testing .

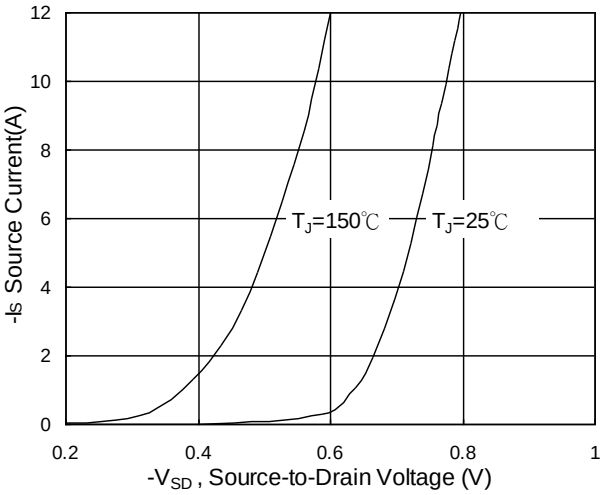
Typical Characteristics



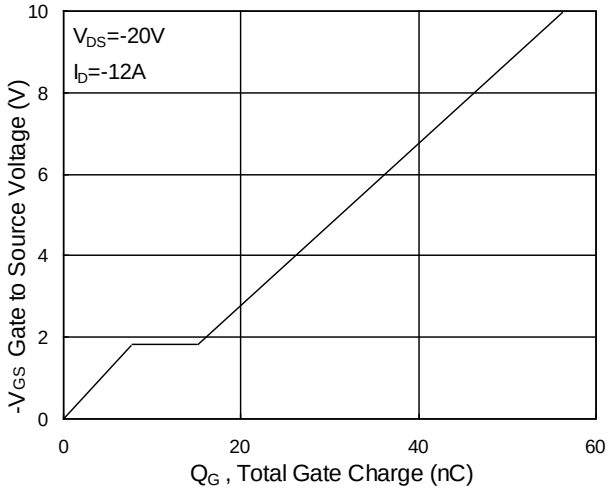
Typical Output Characteristics



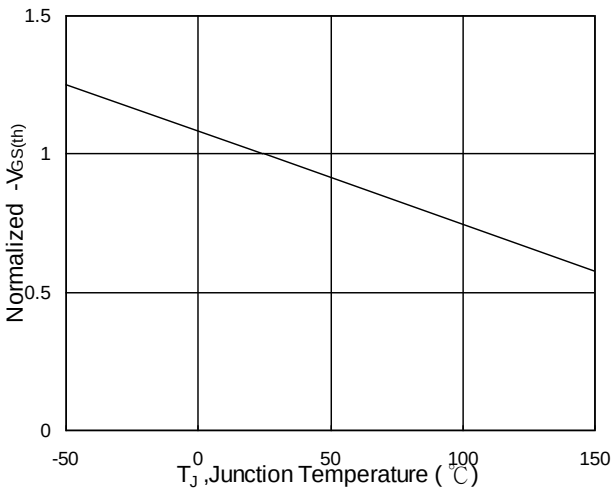
On -Resistance vs G-S Voltage



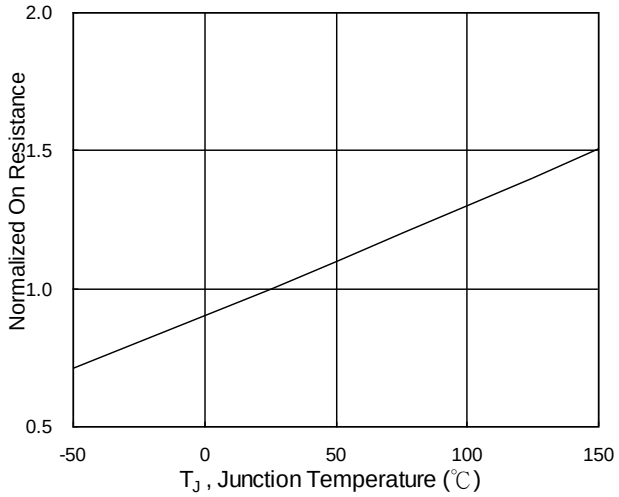
Source Drain Forward Characteristics



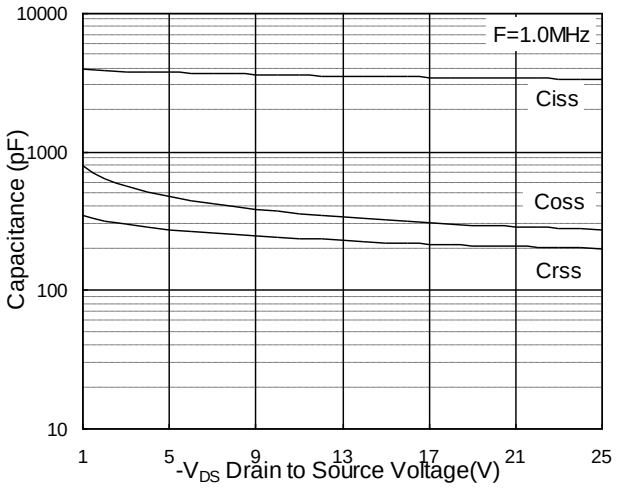
Gate-Charge Characteristics



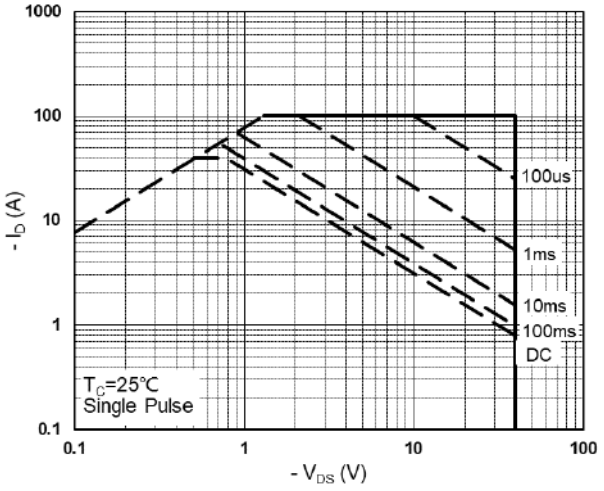
Normalized $V_{GS(th)}$ vs T_J



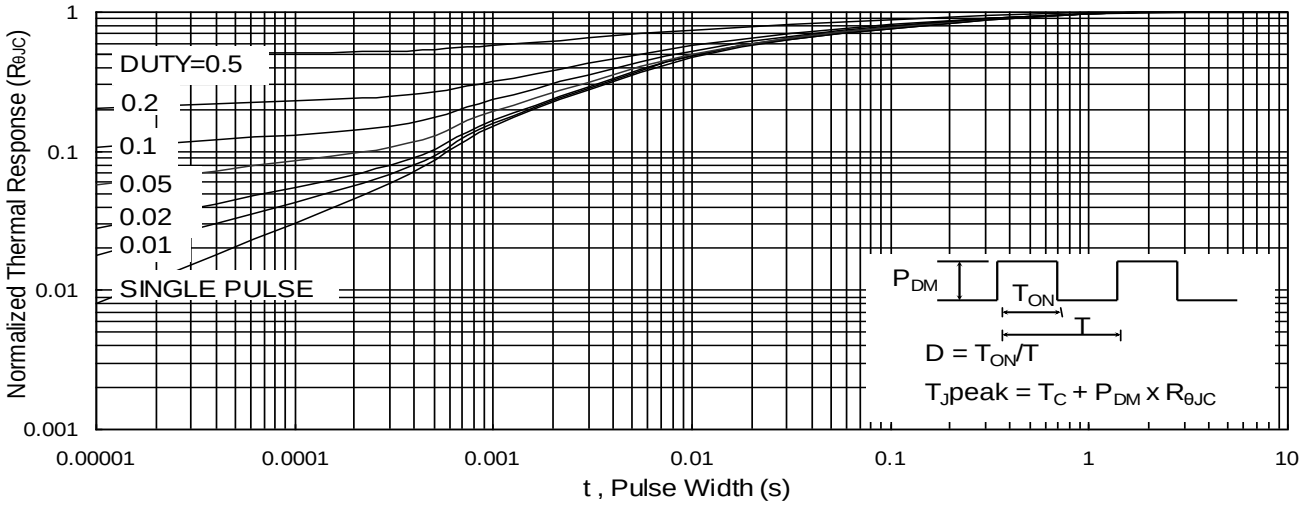
Normalized R_{DSON} vs T_J



Capacitance



Safe Operating Area



Normalized Maximum Transient Thermal Impedance