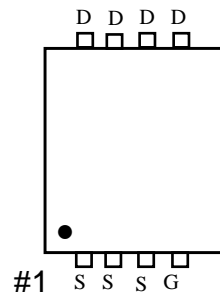


# N-Channel High Density Trench MOSFET

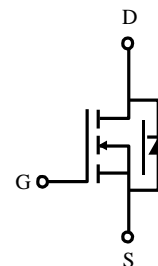
## FEATURES

- Super high dense cell trench design for low  $R_{DS(on)}$ .
- Rugged and reliable.
- Surface Mount package.

PDFN3x3



PRODUCT SUMMARY		
$V_{(BR) DSS}$	$R_{DS(ON)}$	$I_D$
100V	8.5m $\Omega$	48A



## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

PARAMETERS TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Source voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain current	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	48
		$T_C = 100\text{ }^\circ\text{C}$	30
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	192	A
Avalanche Current	$I_{AS}$	20	
Avalanche Energy	$L=0.1\text{mH}$ $E_{AS}$	20	mJ
Power Dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	36
		$T_C = 100\text{ }^\circ\text{C}$	14
Operating junction & Storage Temperature Range	$T_s T_{stg}$	-55 to 150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta Jc}$		3.5	$^\circ\text{C}$
Junction-to-Ambient	$R_{\theta JA}$		75	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$  unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	
Gate - Body Leakage	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$			1	$\mu A$
		$V_{DS}=80V, V_{GS}=0V, T_J=125\text{ }^\circ\text{C}$			30	
Drain - Source On - State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$		8.5	10	m $\Omega$
		$V_{GS}=6V, I_D=20A$		12	15.5	
Forward Trans conductance <sup>1</sup>	$g_{fs}$	$V_{DS}=5V, I_D=10A$		20		S

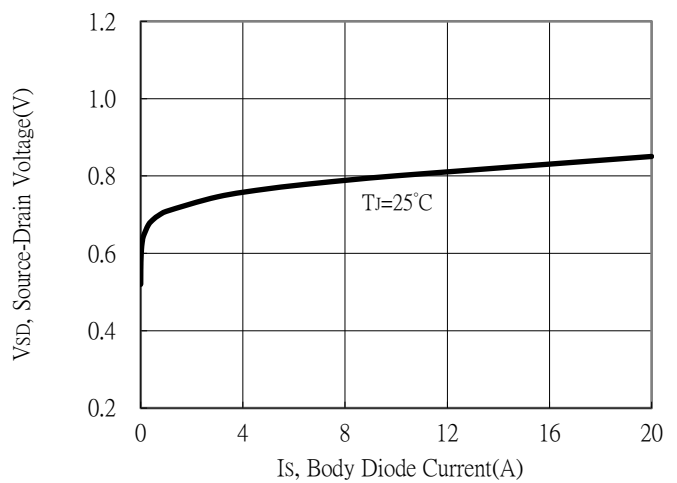
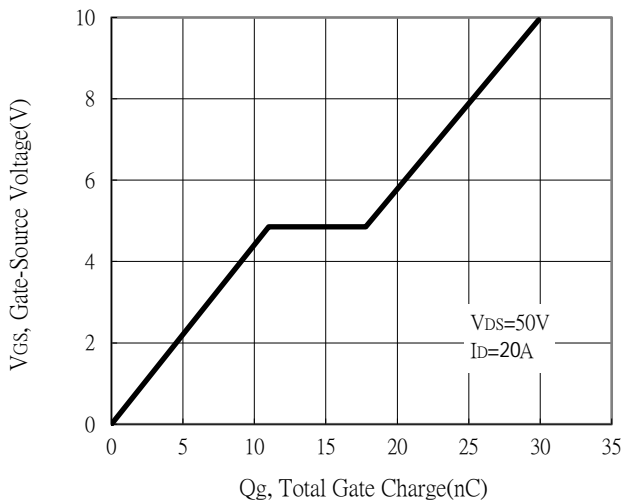
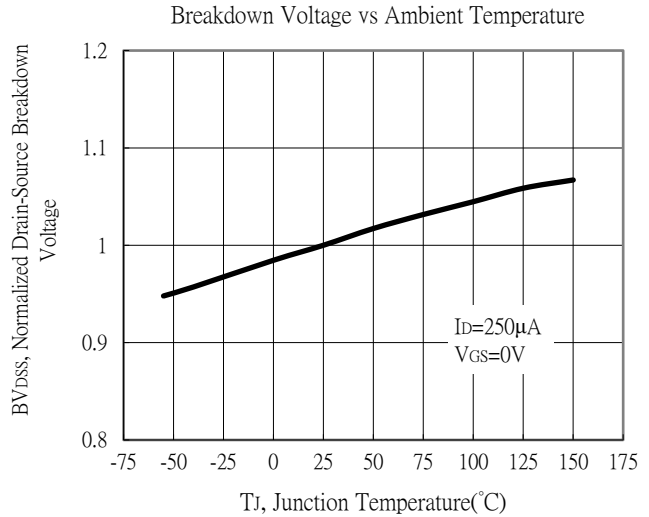
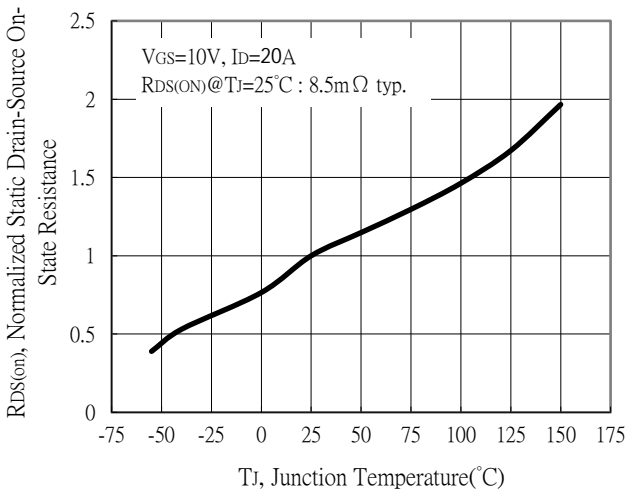
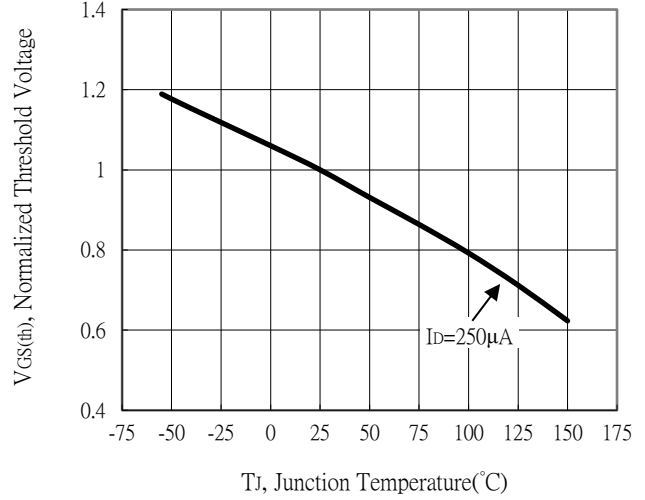
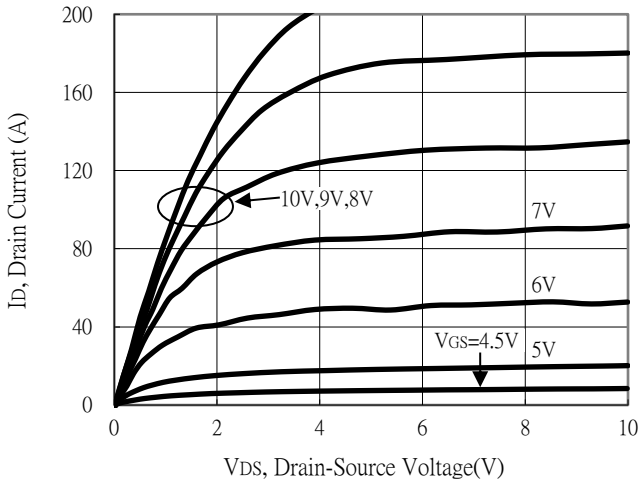
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=50V, f=1MHz$		1560		pF
Output Capacitance	$C_{oss}$			525		
Reverse Transfer Capacitance	$C_{rss}$			55		
Gate Resistance	$R_G$	$V_{GS}=0V, f=1MHz$		0.9		$\Omega$
Total Gate Charge <sup>2</sup>	$Q_{g(vgs=10V)}$	$V_{DS}=50V_{(BR)DSS},$ $I_D = 20A$		30.1		nC
	$Q_{g(vgs=6V)}$			20		
Gate Source Charge <sup>2</sup>	$Q_{gS(VGS=10V)}$			8.8		
	$Q_{gS(VGS=6V)}$			5.7		
Gate-Drain Charge <sup>2</sup>	$Q_{gd(VGS=10V)}$			8.8		
	$Q_{gd(VGS=6V)}$			5.5		
Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$	$V_{DS}=30V,$ $I_D=20A, V_{GS}=10V, R_{GS}=6\Omega$		10.4		nS
Rise Time <sup>2</sup>	$t_r$			17.5		
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$			26.5		
Fall Time <sup>2</sup>	$t_f$			68.9		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS** ( $T_J=25\text{ }^\circ\text{C}$ )

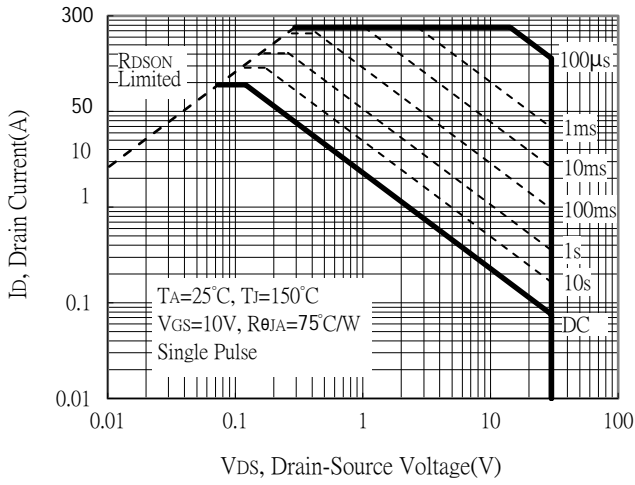
Continuous Current	$I_S$			36		A
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F=I_S, V_{GS}=0V$		0.85	1.2	V
Reverse Recovery Time	$T_{rr}$	$I_F=20A, dI_F/dt=100A/\mu s$		51		nS
Reverse Recovery Charge	$Q_{rr}$			40		nC

Note  
 b. Pulse Test Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .  
 c. Independent of operating production testing.

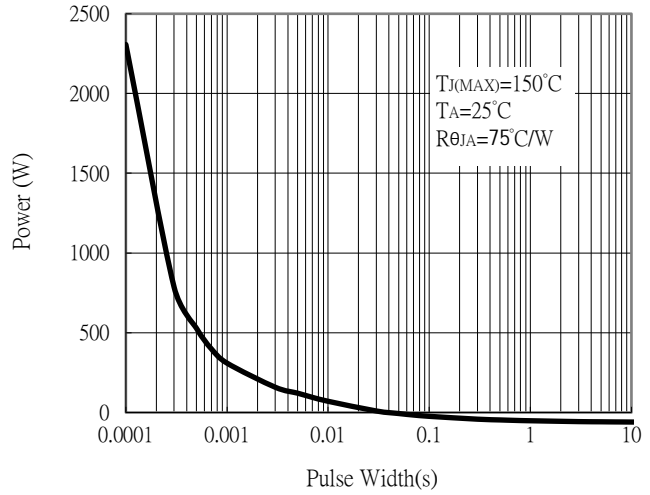
Typical Output Characteristics



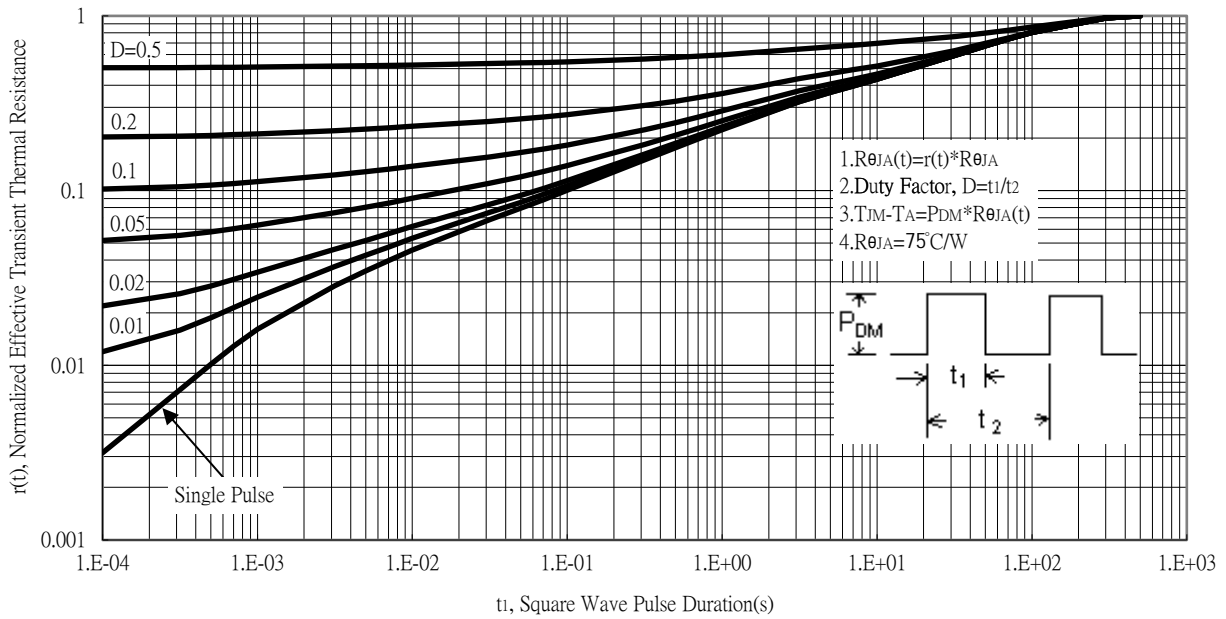
Maximum Safe Operating Area



Single Pulse Power Rating, Junction to Ambient



Transient Thermal Response Curves



Transient Thermal Response Curve