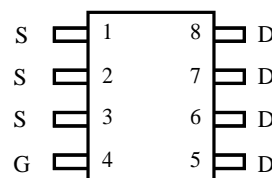


## P -Channel High Density Trench MOSFET

### Features:

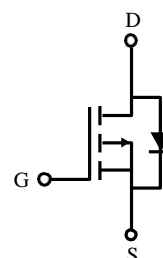
- Super high dense cell trench design for low RDS(on).
- Rugged and reliable.
- Surface Mount package.

SOP-8



### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(on)}$ (m $\Omega$ ) Max	$I_D$
-30V	18 @ $V_{GS} = -10V$	-16A
	30 @ $V_{GS} = -4.5V$	



### ABSOLUTE MAXIMUM RATINGS (TA = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Drain Current-Continuous (Note 1)	$I_D$	$T_A = 25\text{ }^\circ\text{C}$	-16
		$T_A = 70\text{ }^\circ\text{C}$	-12
Pulse Drain Current (Note 2)	$I_{DM}$	-60	A
Avalanche Current	$I_{AS}$	-20	
Single Pulse Avalanche Energy	$E_{AS}$	60	mJ
Maximum Power Dissipation (Note 1)	$P_D$	$T_A = 25\text{ }^\circ\text{C}$	3.1
		$T_A = 75\text{ }^\circ\text{C}$	2.0
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case (Note 1)	$R_{thJC}$	6	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{thJA}$	40	$^\circ\text{C/W}$

Note:

1. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
2. Pulse width limited by maximum junction temperature

**ELECTRICAL CHARACTERISTICS (TA = 25 °C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V , I <sub>D</sub> = -250uA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -24V , V <sub>GS</sub> = 0V , T <sub>j</sub> = 25°C			-1	uA
		V <sub>DS</sub> = -20V , V <sub>GS</sub> = 0V , T <sub>j</sub> = 125°C			-30	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V , V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS (Note 3)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250uA	-1	-2	-3	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V , I <sub>D</sub> = -12A		14.8	18	mΩ
		V <sub>GS</sub> = -4.5V , I <sub>D</sub> = -9A		25	30	mΩ
Forward Transconductance	gfs	V <sub>DS</sub> = -10V , I <sub>D</sub> = -12A		28		S
<b>DYNAMIC CHARACTERISTICS (Note 4)</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -15V , V <sub>GS</sub> = 0V f = 1.0MHz			1012	pF
Output Capacitance	C <sub>OSS</sub>				214	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>				151	pF
<b>SWITCHING CHARACTERISTICS (Note 4)</b>						
Turn-On Delay Time	td <sub>(ON)</sub>	V <sub>DD</sub> = -15V , I <sub>D</sub> = -1A V <sub>GS</sub> = -10V R <sub>GS</sub> = 6 Ω		8.0		nS
Rise Time	tr			12		nS
Turn-Off Delay Time	td <sub>(OFF)</sub>			32		nS
Fall Time	tf			16		nS
Total Gate Charge (10V)	Qg	V <sub>DS</sub> = -15V , I <sub>D</sub> = -12A V <sub>GS</sub> = -10V		21.0		nC
Total Gate Charge (4.5V)	Qg			12.0		nC
Gate-Source Charge	Qgs			2.6		nC
Gate-Drain Charge	Qgd			6.2		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Drain-Source Diode Forward Current (Note 1)	I <sub>S</sub>			-2.8		A
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> = 0V , I <sub>F</sub> = I <sub>S</sub>		-0.7	-1	V

Note:

3. Pulse Test Pulse width ≤ 300us, Duty Cycle ≤ 2% .

4. Guaranteed by design , not subject to production testing .

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

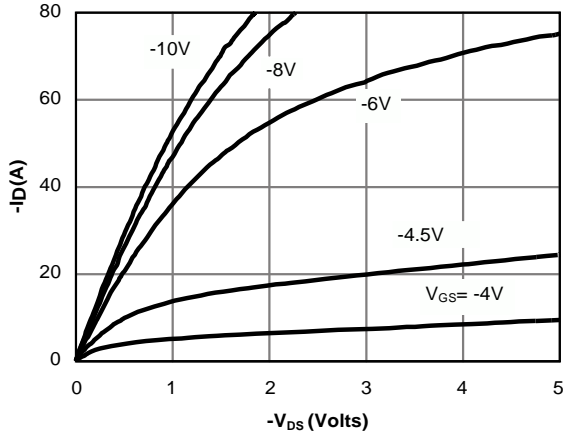


Figure 1: On-Region Characteristics

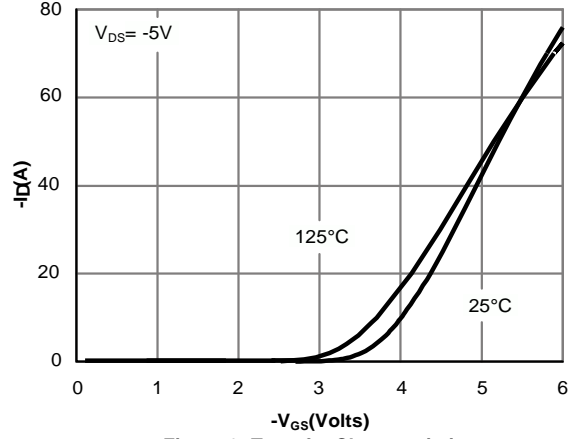


Figure 2: Transfer Characteristics

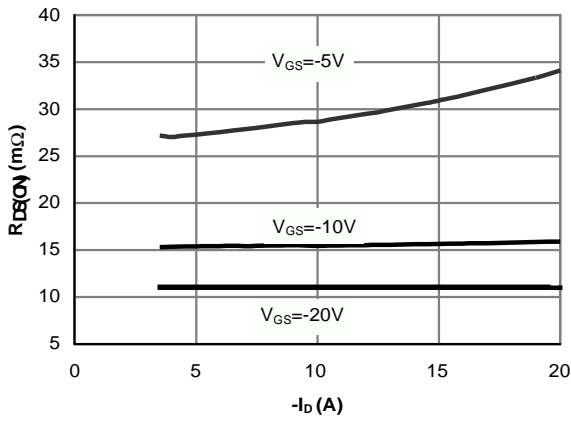


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

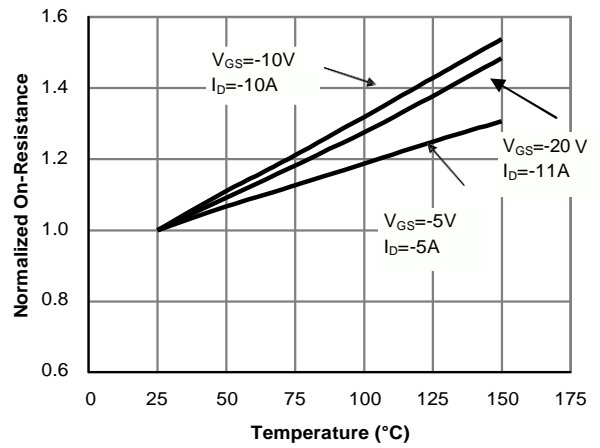


Figure 4: On-Resistance vs. Junction Temperature

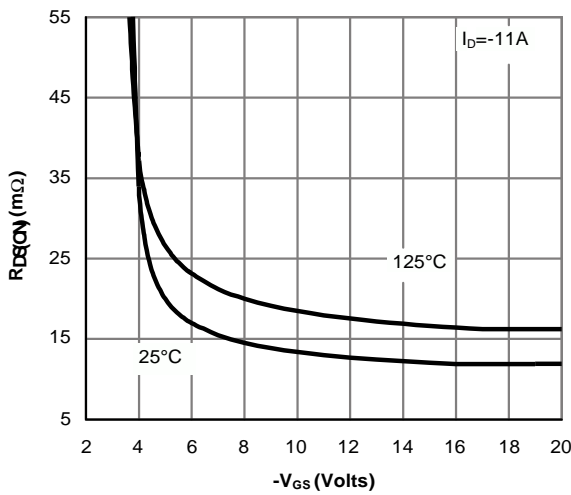


Figure 5: On-Resistance vs. Gate-Source Voltage

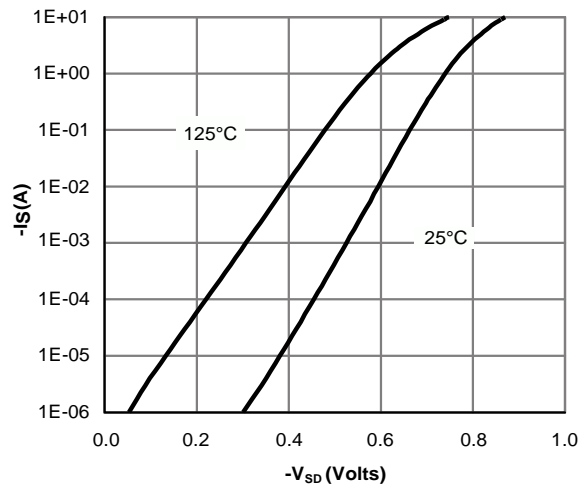


Figure 6: Body-Diode Characteristics

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

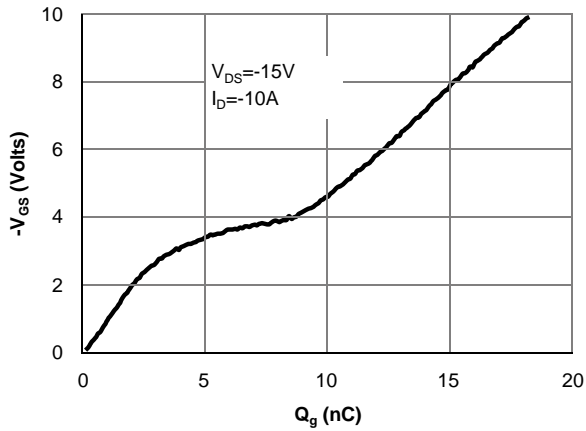


Figure 7: Gate-Charge Characteristics

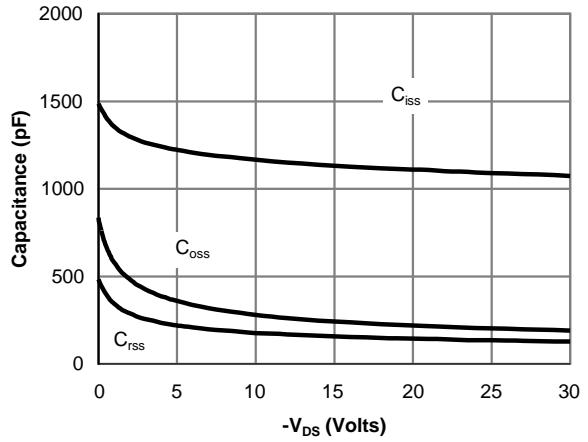


Figure 8: Capacitance Characteristics

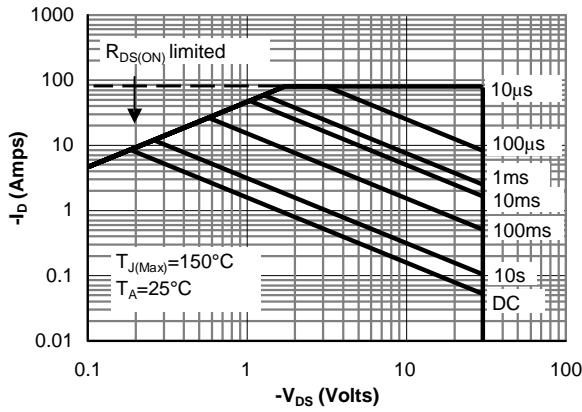


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

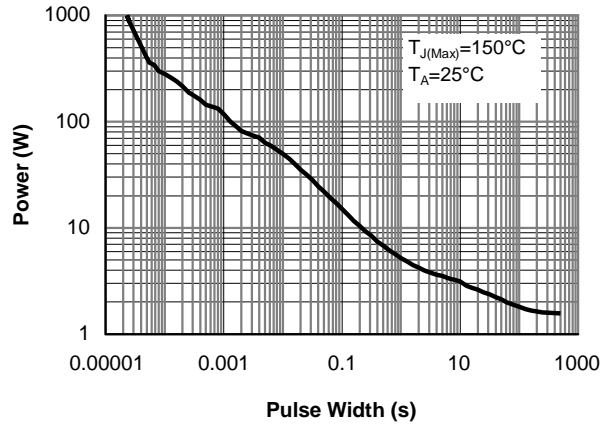


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

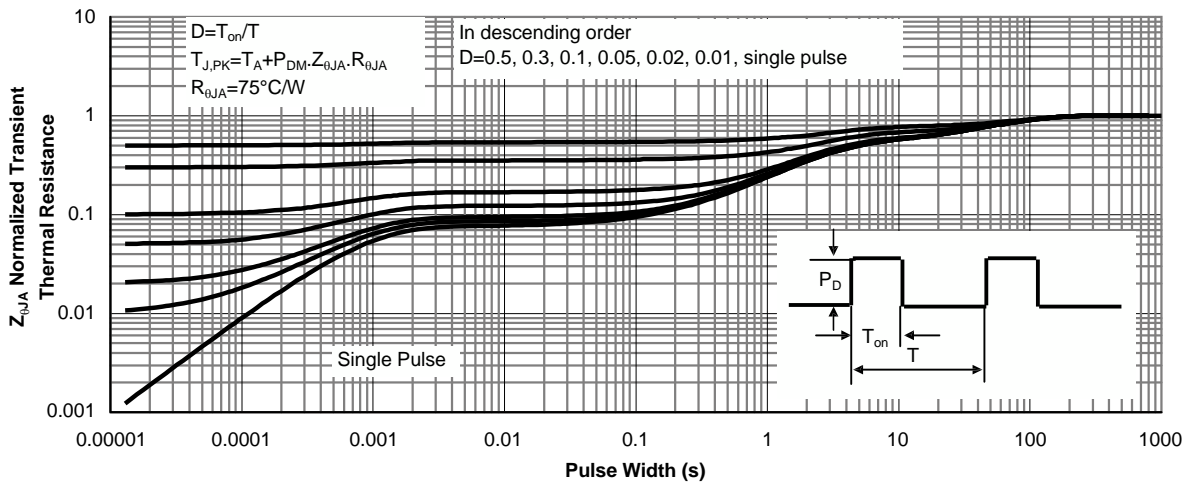
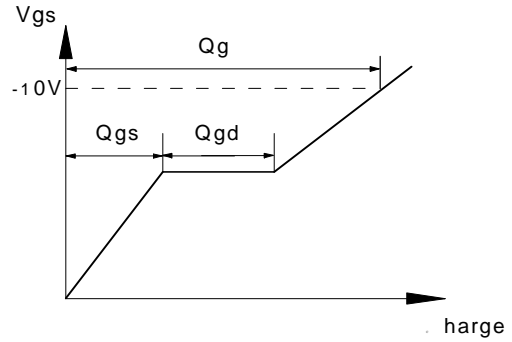
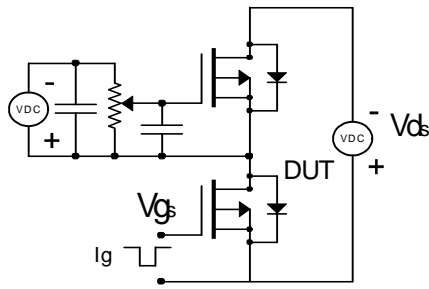
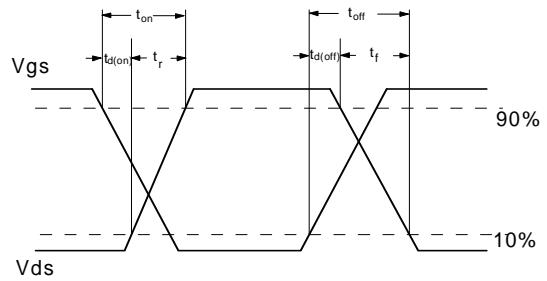
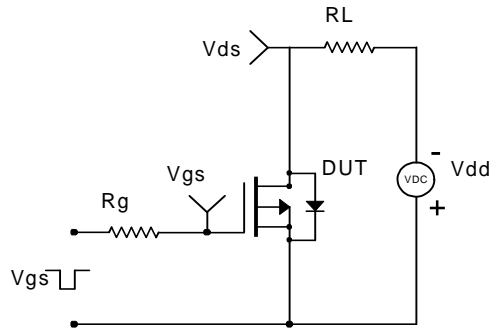


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

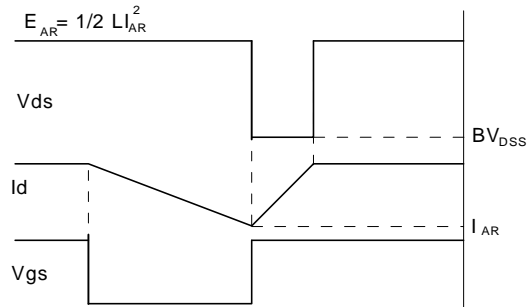
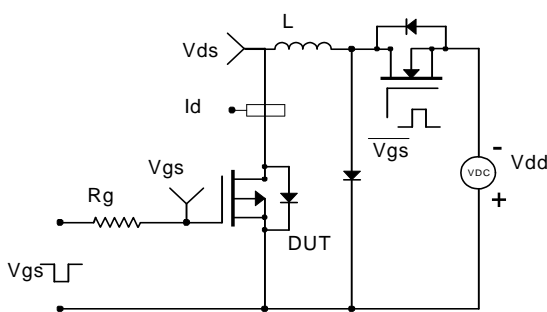
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

