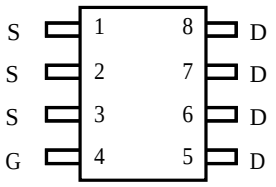
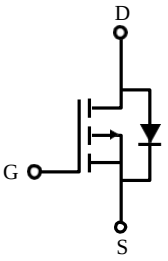
P -Channel High Density TrenchMOSFET

Features:

- Super high dense cell trench design for low RDS(on).
- Rugged and reliable.
- Surface Mount package.

SOP-8





PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(on)}$ (mΩ) Max	I_D
-30V	23 @ V_{GS} = -10V	-15A
	33 @ V_{GS} = -4.5V	

ABSOLUTE MAXIMUM RATINGS (TA = 25 ℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuousa (Note 1)	T_A = 25 ℃	I_D	-15	A
	T_A = 70 ℃		-12	
Pulse Drain Current(Note 2)		I_{DM}	-50	
Avalanche Current		I_{AS}	-16	
Single Pulse Avalanche Energy	L=0.1mH	E_{AS}	48	mJ
Maximum Power Dissipation (Note 1)	T_A=25℃	P_D	3.1	W
	T_A=75℃		2.0	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	- 55 to 150	℃

THERMAL CHARACTERISTICS

Thermal Resistance,Junction-to-Case (Note 1)	R_{thJC}	6	℃/W
Thermal Resistance,Junction-to-Ambient (Note 1)	R_{thJA}	40	℃/W

Note：

1. Surface Mounted on FR4 Board , t ≤ 10sec.
2. Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (TA = 25 ℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V , I_D = -250uA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V , V_{GS} = 0V, Tj = 25℃			-1	uA
		V_{DS} = -20V , V_{GS} = 0V , Tj = 125℃			-30	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V , V_{DS} = 0V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = -250uA	-1	-2	-3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10V , I_D = -12A		17.5	23	mΩ
		V_{GS} = -4.5V , I_D = -8A		22.5	33	mΩ
Forward Transconductance	gfs	V_{DS} = -10V , I_D = -12A		18		S
DYNAMIC CHARACTERISTICS (Note 4)						
Input Capacitance	C_{ISS}	V_{DS} = -15V , V_{GS} = 0V f = 1.0MHz			2398	pF
Output Capacitance	C_{OSS}				296	pF
Reverse Transfer Capacitance	C_{RSS}				148	pF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	$td_{(ON)}$	V_{DD} = -15V , I_D = -1A V_{GS} = -10V R_{GS} = 6 Ω		8.0		nS
Rise Time	tr			12		nS
Turn-Off Delay Time	$td_{(OFF)}$			32		nS
Fall Time	tf			16		nS
Total Gate Charge (10V)	Qg	V_{DS} = -15V , I_D = -12A V_{GS} = -10V		27.0		nC
Total Gate Charge (4.5V)	Qg			12.6		nC
Gate-Source Charge	Qgs			6.7		nC
Gate-Drain Charge	Qgd			4.1		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Drain-Source Diode Forward Current (Note 1)	I_S			-4.5		A
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS} = 0V , I_F = I_S		-0.7	-1.3	V

Note：
3. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2% .
4. Guaranteed by design , not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

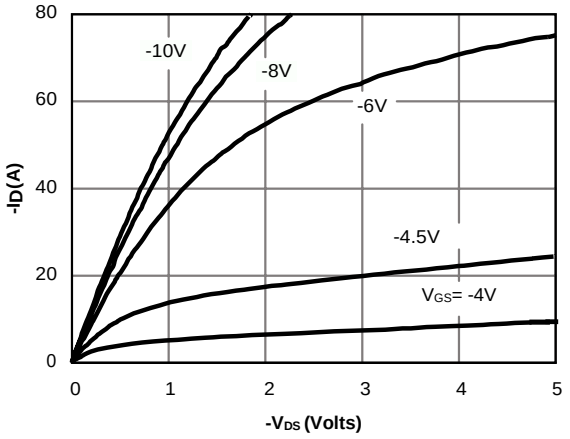


Figure 1: On-Region Characteristics

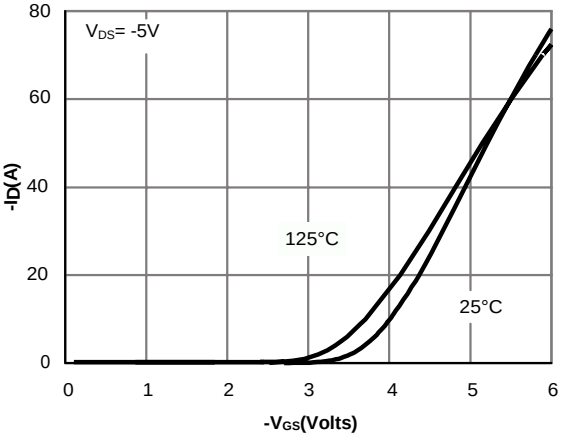


Figure 2: Transfer Characteristics

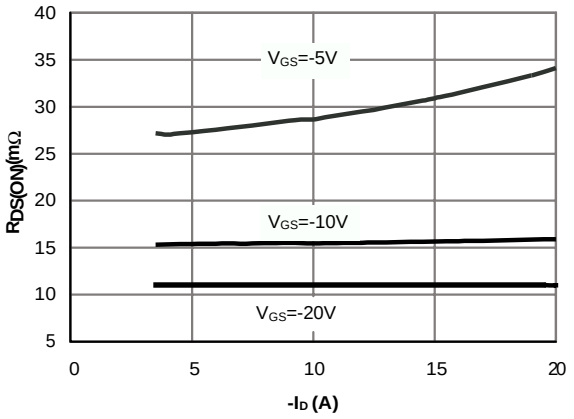


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

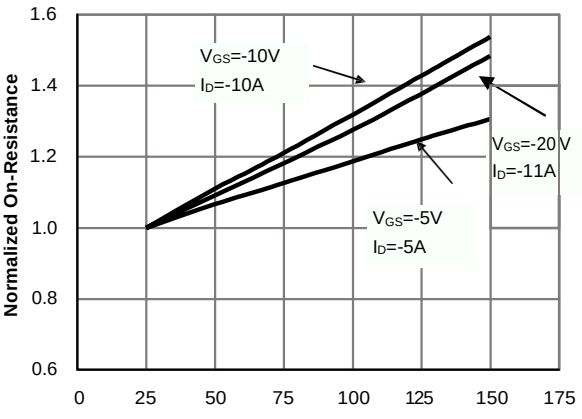


Figure 4: On-Resistance vs. Junction Temperature

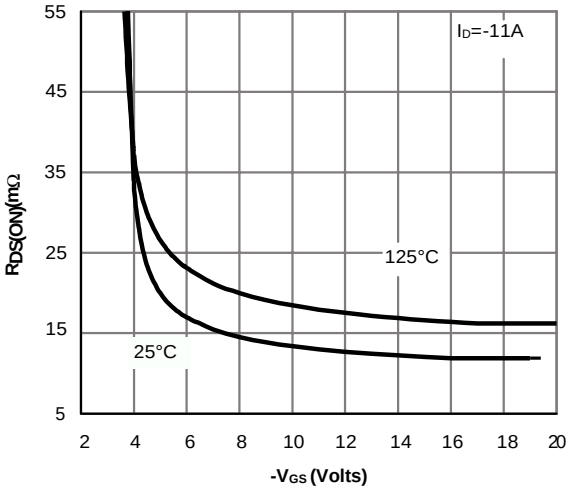


Figure 5: On-Resistance vs. Gate-Source Voltage

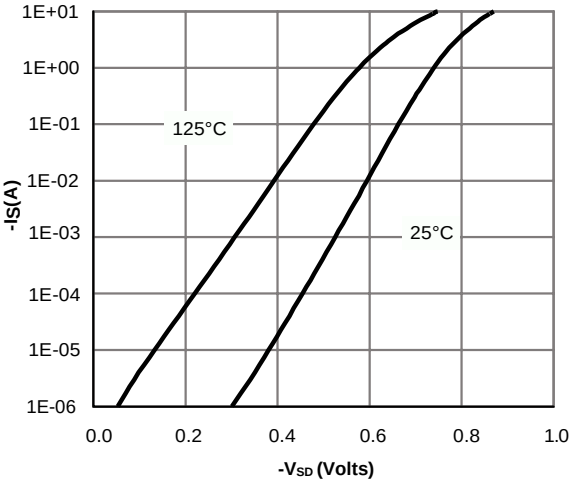


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

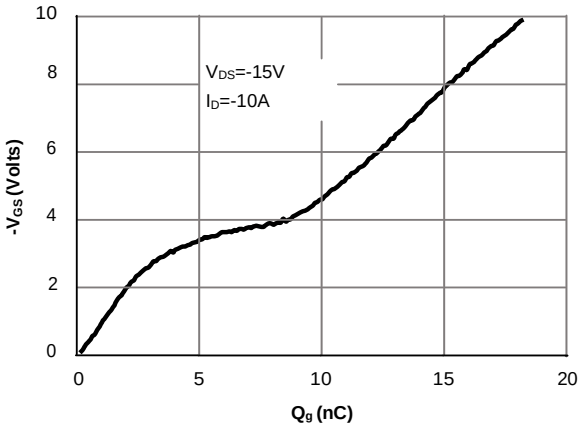


Figure 7: Gate-Charge Characteristics

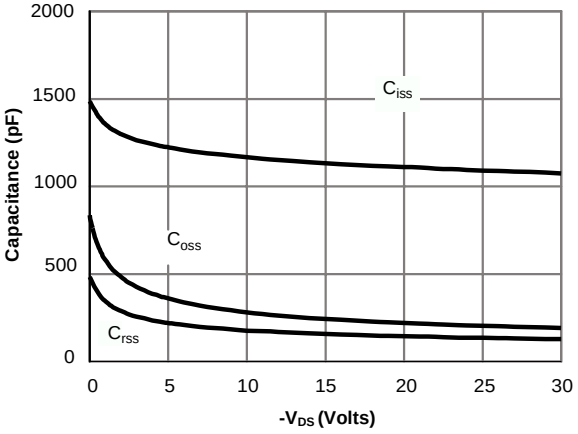


Figure 8: Capacitance Characteristics

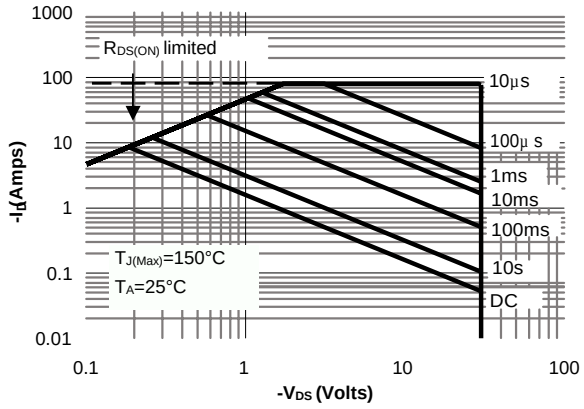


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

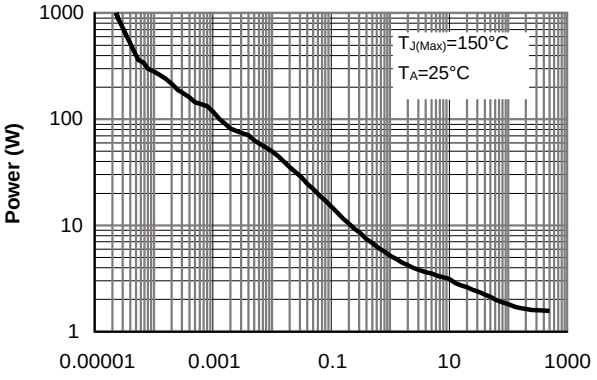


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

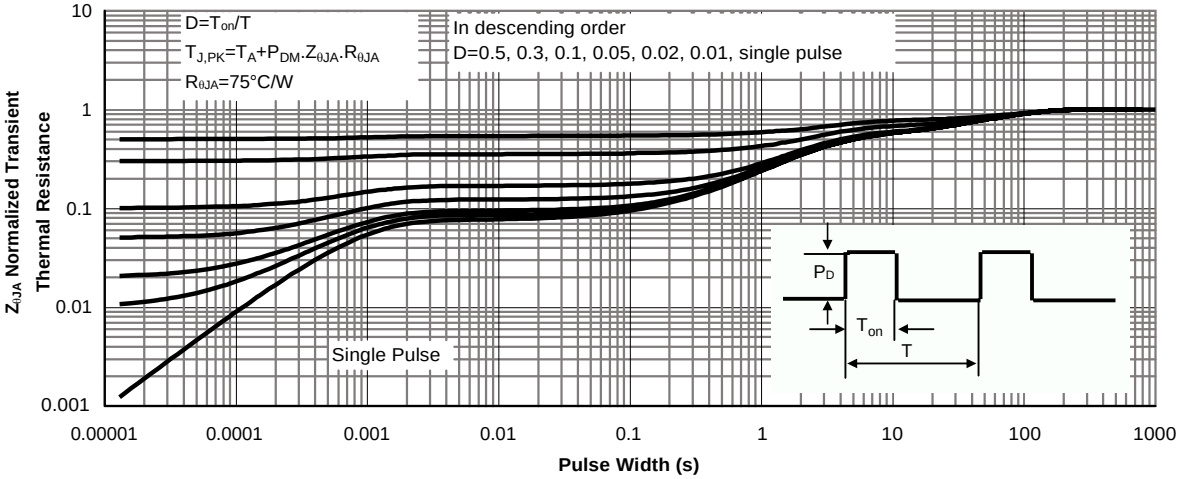
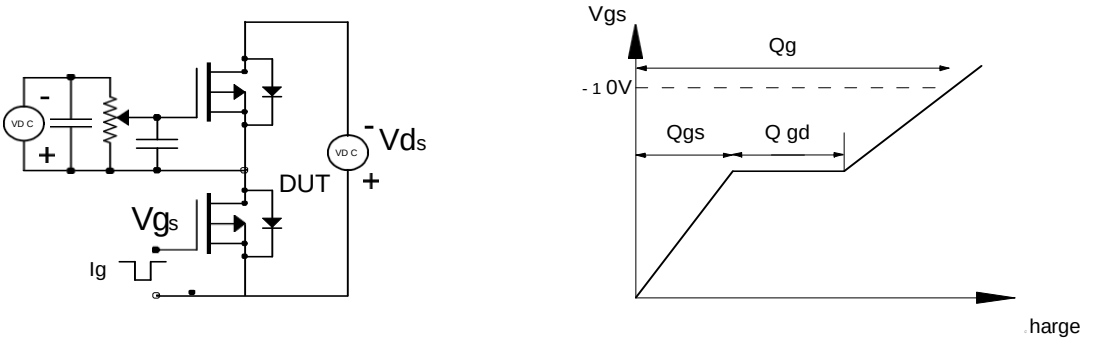
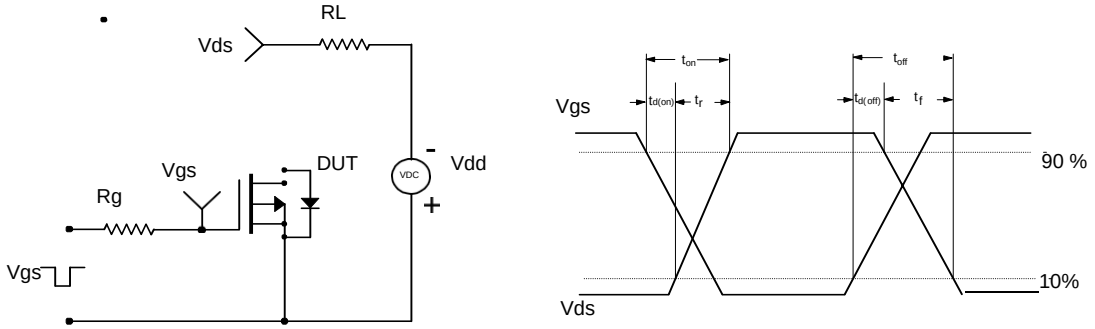


Figure 11: Normalized Maximum Transient Thermal Impedance(Note E)

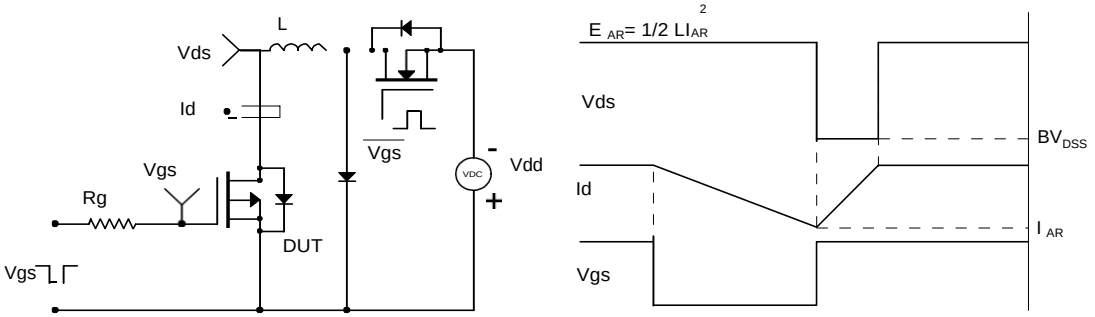
G ate C harge Test C ircuit & W aveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & W aveforms



Diode Recovery Test Circuit & W aveforms