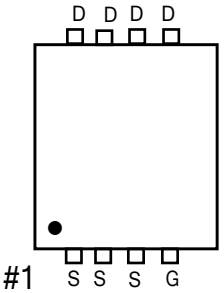
N-Channel High Density Trench MOSFET

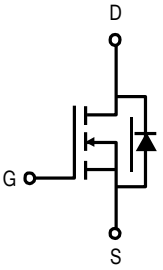
PDFN5x6



Features:

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

V (BR) DSS	RDS (ON)	I D
60V	4.4m Ω	80A

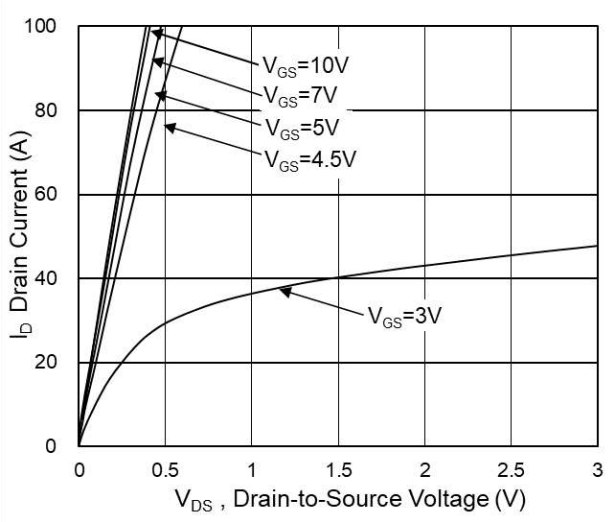


PARAME TERS TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gata-Source voltage		VGS	±20	V
Continuous Drain current	TC = 25℃	ID	80	A
	TC = 100 ℃		52	
Puised Drain Current[1]		IDM	300	
Avalanche Current		IAS	42	
Avalanche Energy	L=0.5mH	EAS	92	mJ
Power Dissipation	TC = 25℃	PD	54.2	W
	TC = 100 ℃		28	
Operaing junction& Storege Temperature Range		TS,TSTG	-55 to 150	℃

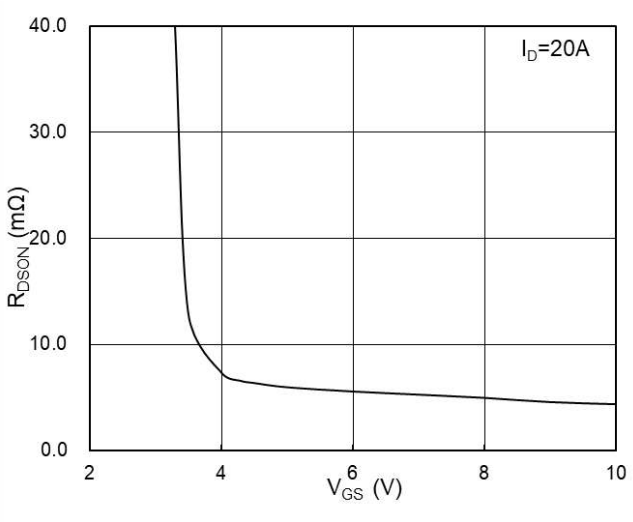
Thermal Resistance	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	RthJC		2.4	℃/W
Junction-Ambient	RthJA		56	℃/W

Parameter	Symbol	TEST CONDITIONS	LIMITS			Unit
			Min	Typ	Max	
STATIC						
Drain-Source Breakdown Voltege Gate	V(BR)DSS	VGS=0V,ID=250μA	60			V
Threshold Voltage	VGS(th)	VDS=VGS,ID=250μA	1	1.6	25	
Gate-Body Leakage	IGSS	VDS=0V,VGS=± 2 0V			±100	nA
Zero Gate Voltage Dain Current	IDSS	VDS=48V,VGS=0 V			1	μA
		VDS=20V,VGS=0V,TJ=125℃			30	
Drain-Source On- State Resistance[1]	RDS(ON)	VGS=4.5V,ID=10A		6.4	7.8	mΩ
		VGS=10V,ID=20A		4.4	5.2	
Forward Trans conductance[1]	gfs	VDS=5V,ID=16A		18		S
DYNAMIC						
Input Capacitance Output	C_{ISS}	VGS=0V,VDS=30V,f=1MHZ		1625		pF
Capacitance	C_{OSS}			438		
Reverse Transfer Capacitance Gate	C_{RSS}			25		
Resistance	Rg	VGS=0V,f=1MHZ		1.3		Ω
Total Gate Charge[2]	Qg(vgs=10V)	VDS=30V (BR)DSS, ID = 2 0A		33.5		nC
	Qg(vgs=4.5V)			17.8		
Gate Source Charge[2]	QgS(VGS=10V)			5.8		
	QgS(VGS=4.5V)			3.9		
Gate-Drain Charge[2]	Qgd(VGS=10V)			7.9		
	Qgd(VGS=4.5V)			5.3		
Tum-On Delay Time[2]	td(on)	VDS=30V,RL=1.5Ω ID=20A,VGS=10V.RGS=3Ω		7.5		nS
Rise Time[2]	tr			6		
Tum-Off Delay Time[2]	td(off)			29		
Fall Time[2]	tr			7.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS(TJ=25℃)						
Continuous Current	IS			60		A
Forward Voltage[1]	VSD	IF=IS,VGS=0V		0.8	1.2	V
Reverse Recovery Time	Trr	IF=20V,d1f/dt=100A/μs		23		nS
Reverse Recovery Charge	Qrr			60		nC

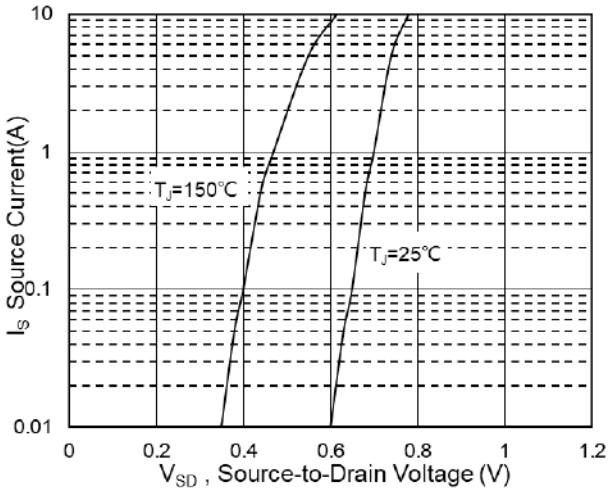
Note
b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .
c. Independent of operating production testing .



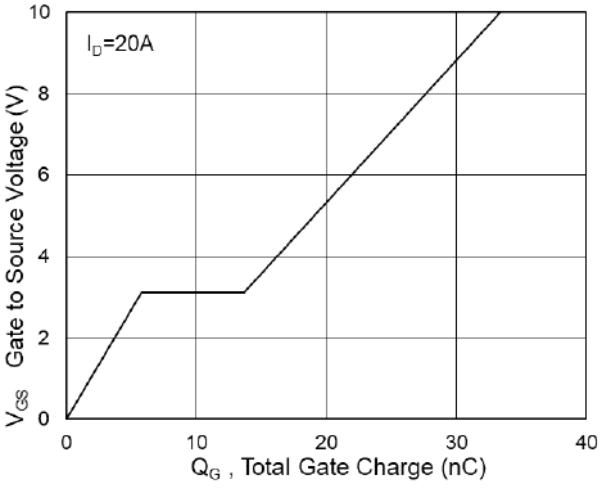
Typical Output Characteristics



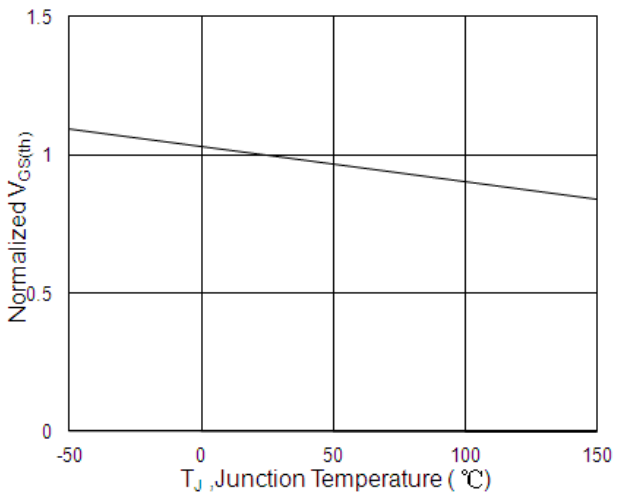
On-Resistance vs G-S Voltage



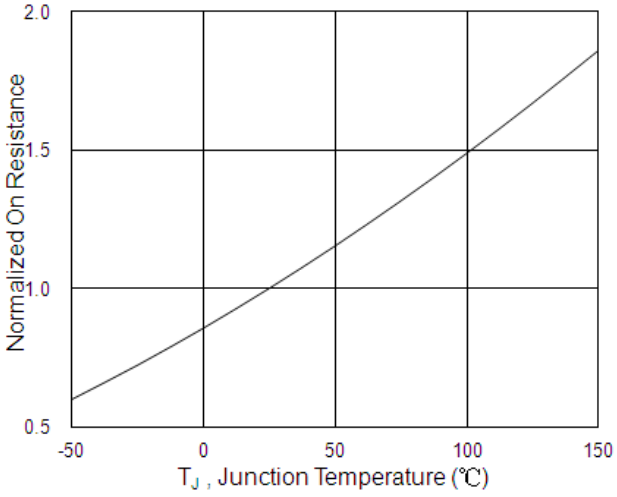
Source Drain Forward Characteristics



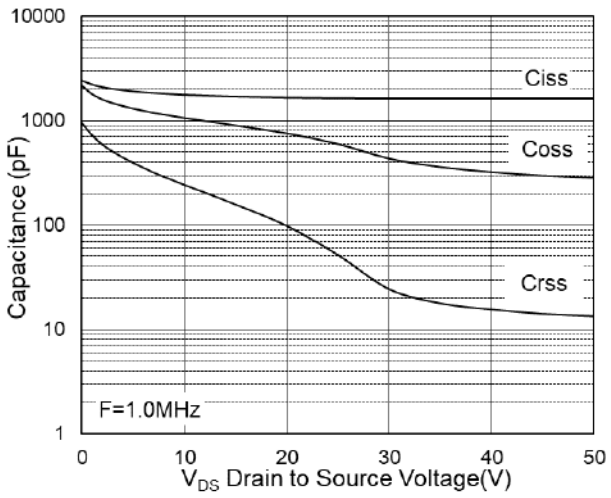
Gate-Charge Characteristics



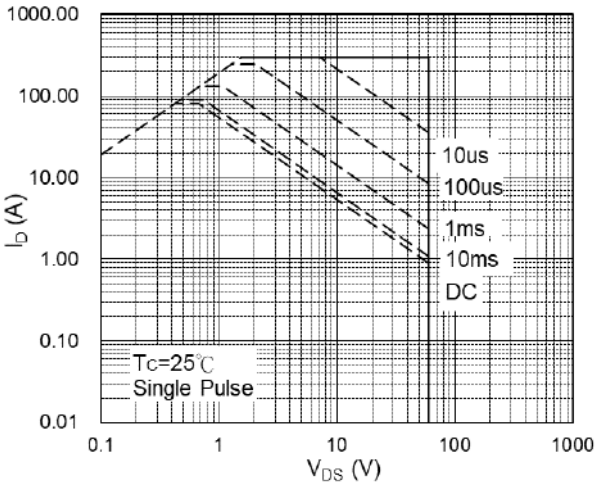
Normalized $V_{GS(th)}$ vs T_J



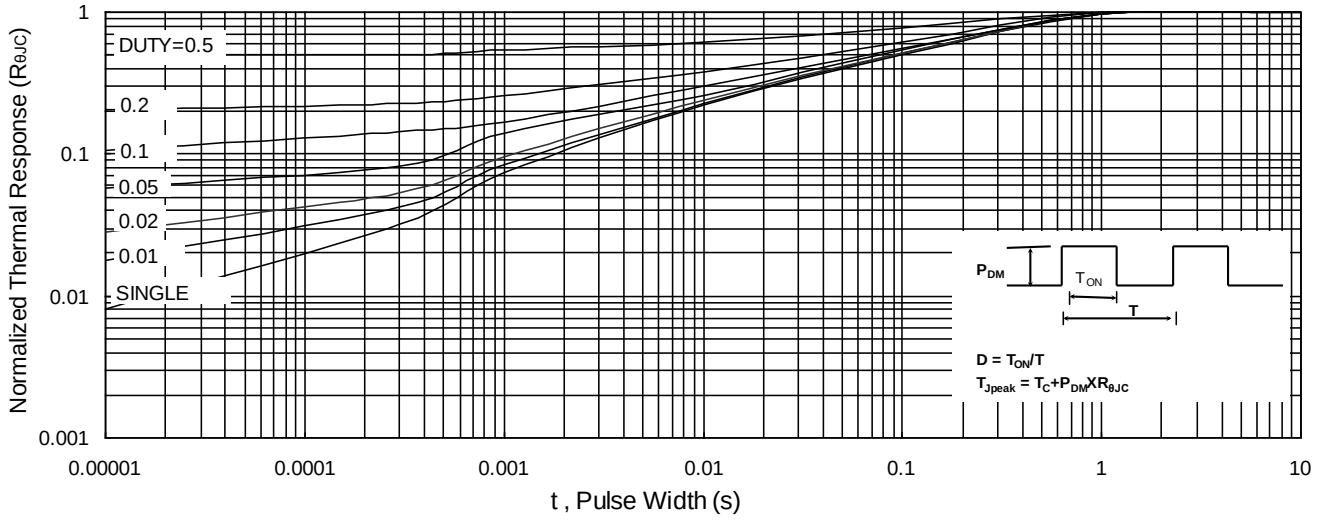
Normalized R_{DSON} vs T_J



Capacitance



Safe Operating Area



Normalized Maximum Transient Thermal Impedance