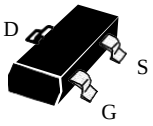
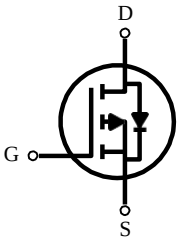
P-Channel High Density Trench MOSFET

Features:

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

SOT-23-3L





PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (mΩ) Max
-60V	- 3.5A	78@ V_{GS} = -10V
	- 2.8A	86 @ V_{GS} = -4.5V

ABSOLUTE MAXIMUM RATINGS (T_A = 25 ℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 60	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous[a] @ T_A = 25 ℃		I_D	- 3.5	A
-Pulse[b]		I_{DM}	- 15	A
Drain-Source Diode Forward Current [a]		I_S	- 2	A
Maximum Power Dissipation [a]	TA=25℃	P_D	1.25	W
	TA=75℃		0.75	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	- 55 to 150	℃

THERMAL CHARACTERISTICS

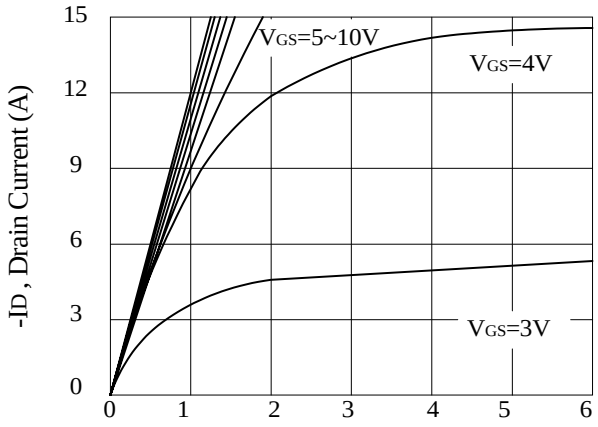
Thermal Resistance,Junction-to-Ambient[a]	R_{thJA}	100	°C/W

Note：
a. Surface Mounted on FR4 Board , t ≤ 5sec .
b. Pulse width limited by maximum junction temperature .

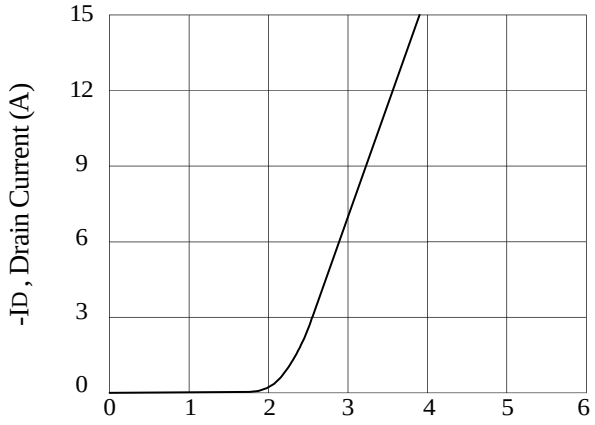
ELECTRICAL CHARACTERISTICS (TA= 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V , I_D = -250uA	-60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48V , V_{GS} = 0V			-1	uA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V , V_{DS} = 0V			-100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = -250uA	-1	-1.5	-3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10V , I_D = -3.5A		63	78	mΩ
		V_{GS} = -4.5V , I_D = -2.8A		70	86	
Forward Transconductance	g_{fs}	V_{DS} = -15V , I_D = -3A		13		S
DRAIN-SOURCE DIODE CHARACTERISTICS[b]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V , I_S = -2A			-1.3	V
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} = -15V , V_{GS} = 0V f = 1.0MHz		1013		pF
Output Capacitance	C_{OSS}			98		pF
Reverse Transfer Capacitance	C_{RSS}			77		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = -15V , I_D = -1A V_{GEN} = -10V R_L = 15 Ω R_{GEN} = 6 Ω		5.8		ns
Rise Time	t_r			3.1		ns
Turn-Off Delay Time	$t_{D(OFF)}$			38		ns
Fall Time	t_f			6.7		ns
Total Gate Charge	Q_g	V_{DS} = -15V I_D = -3.5A V_{GS} = -10V		24		nC
Gate-Source Charge	Q_{gs}			3.7		nC
Gate-Drain Charge	Q_{gd}			3.3		nC

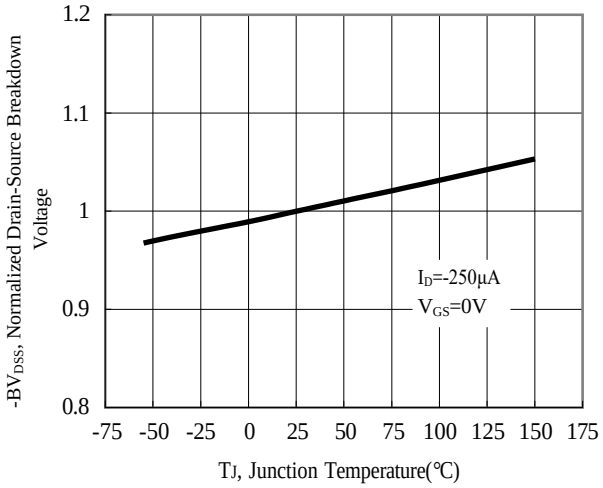
Note：
b. Pulse：Pulse width ≤ 300us , Duty Cycle ≤ 2% .
c. Guaranteed by design , not subject to production testing .

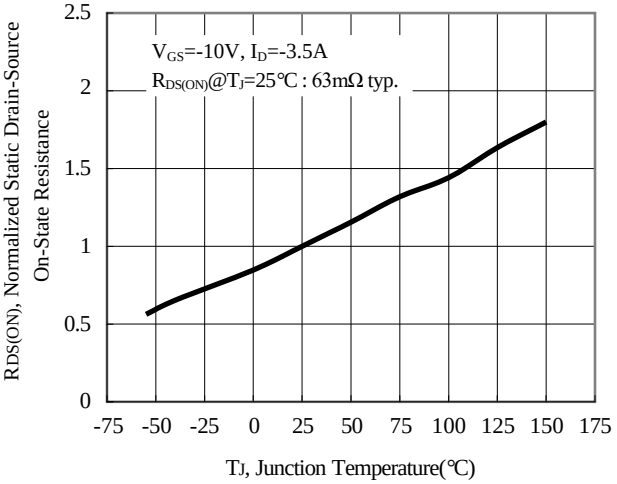


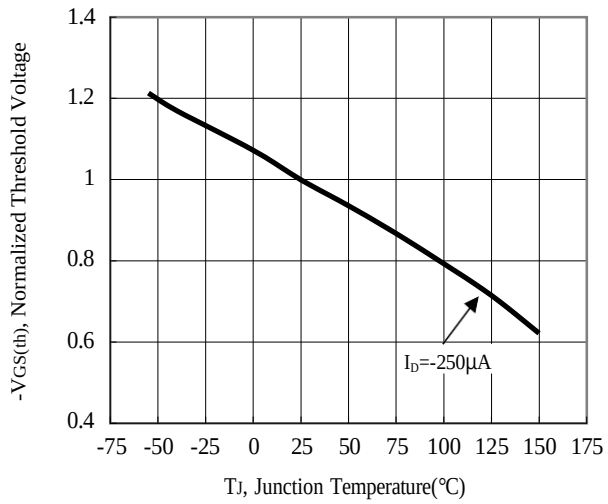
Output Characteristics

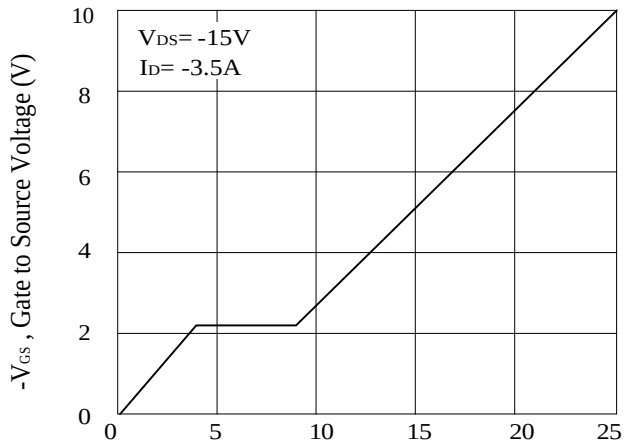


Transfer Characteristics

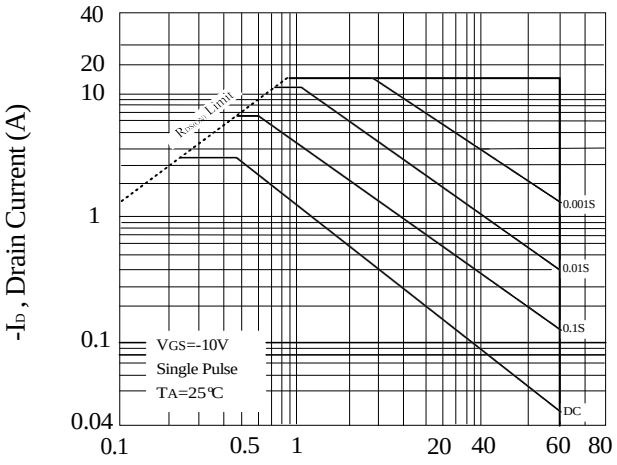




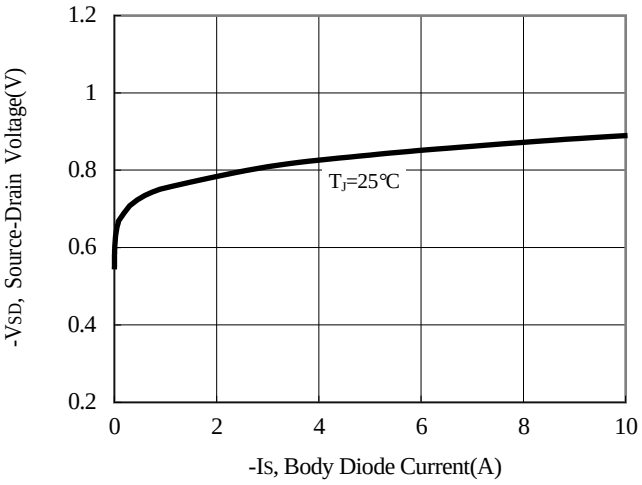


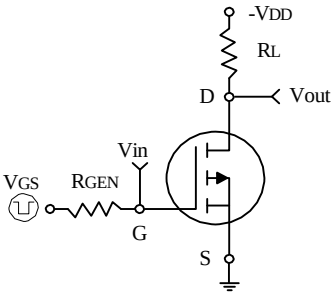


Gate Charge



-VDS , Drain-Source Voltage (V)
Maximum Safe Operating Area





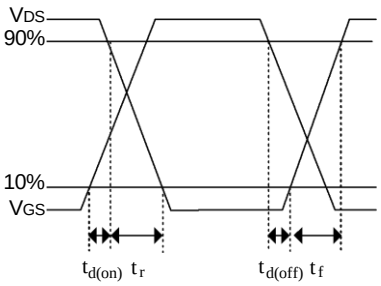
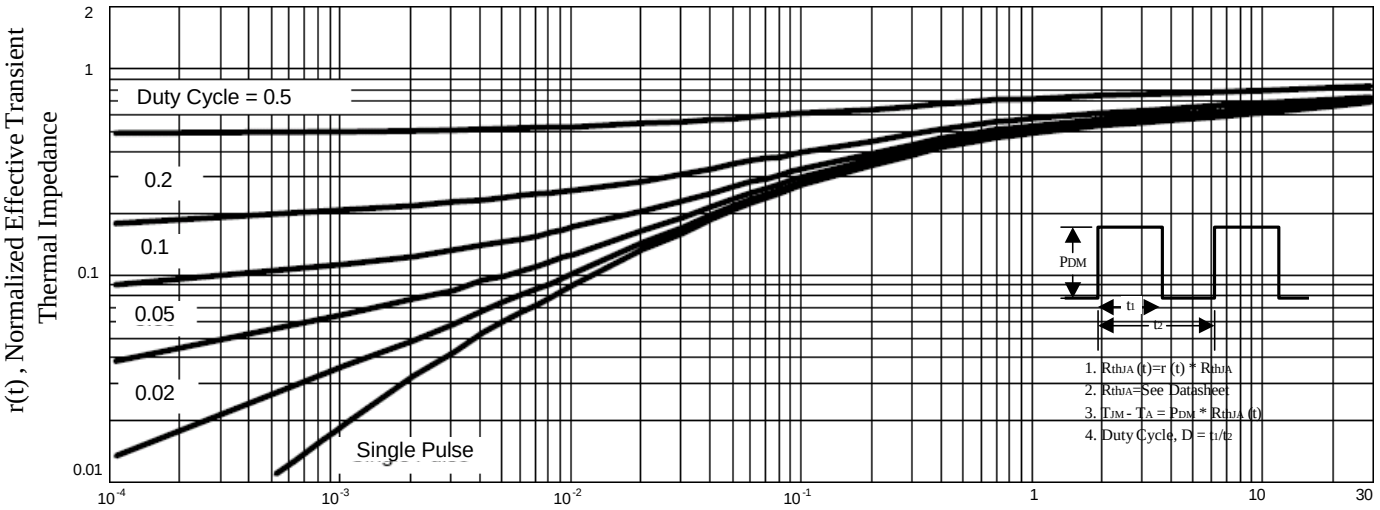


Figure 9. Switching Test Circuit and Switching Waveforms



Square Wave Pulse Duration (sec)
Normalized Thermal Transient Impedance Curve