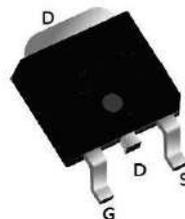


N-Channel High Density Trench MOSFET

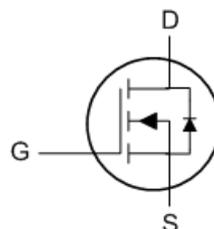
Features:

- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



PRODUCT SUMMARY

V _{DSS}	R _{DS(on)} (m-ohm) Max	I _D
100V	100 @ V _{GS} = 10V	14.6 A
	110 @ V _{GS} = 4.5V	



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous ¹	I _D	T _c =25°C	14.6
		T _c =100°C	10
Pulsed Drain Current ²	I _{DM}	25	A
Single Pulse Avalanche Energy ³	EAS	0.8	mJ
Avalanche Current	I _{AS}	4	A
Maximum Power Dissipation	P _D	30.0	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ¹	R _{thJA}	50	°C/W
Thermal Resistance, Junction-to-Case ¹	R _{thJC}	3	°C/W

ELECTRICAL CHARACTERISTICS (TA = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V, T_j = 25^\circ C$			10	uA
		$V_{DS} = 80V, V_{GS} = 0V, T_j = 55^\circ C$			100	
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	1.2		2.9	V
Drain-Source On-State Resistance ²	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 3A$			110	m Ω
		$V_{GS} = 10V, I_D = 5A$			100	m Ω
Gate Resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		3		Ω
Forward Transconductance	g_{fs}	$V_{DS} = 5V, I_D = 5A$		14.0		S
DRAIN-SOURCE DIODE CHARACTERISTICS						
Continuous Current ^{1,5}	I_S	$V_G=V_D=0V, \text{Force Current}$			14.6	A
Pulsed Source Current ^{2,5}	I_{SM}				25	A
Diode Forward Voltage ²	V_{SD}	$V_{GS} = 0V, I_S = 1A$			1.2	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iSS}	$V_{DS}=15V, V_{GS}=0V$ $f = 1.0MHz$		450		pF
Output Capacitance	C_{OSS}			55		pF
Reverse Transfer Capacitance	C_{RSS}			16		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD}=50V, V_{GS}=10V, R_G=3\Omega, I_D=5A$		3.8		ns
Rise Time	t_r			25.8		ns
Turn-Off Delay Time	$t_{d(OFF)}$			16		ns
Fall Time	t_f			8.8		ns
Total Gate Charge	$Q_g(V_{GS}=10V)$	$V_{DS}=50V, V_{GS}=10V, I_D=5A$		11.9		nC
Gate-Source Charge	Q_{gs}			2.8		nC
Gate-Drain Charge	Q_{gd}			1.7		nC

Note:

- The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=4A$
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation

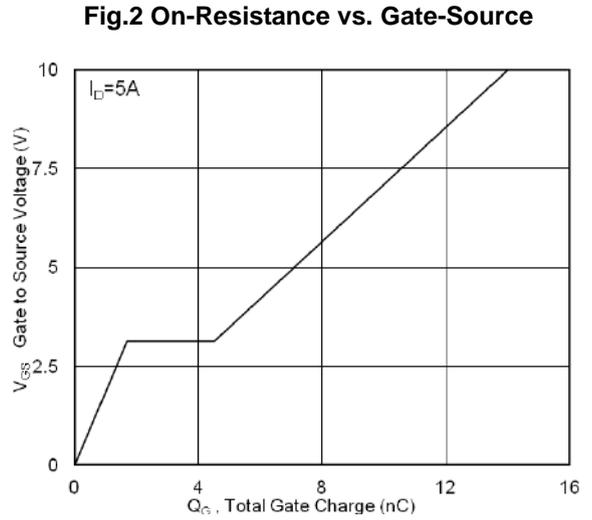
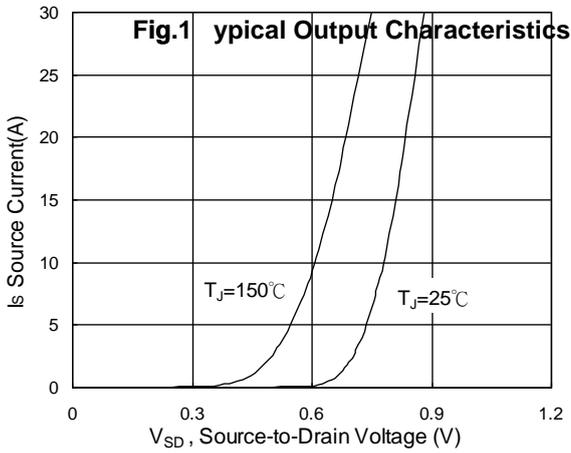
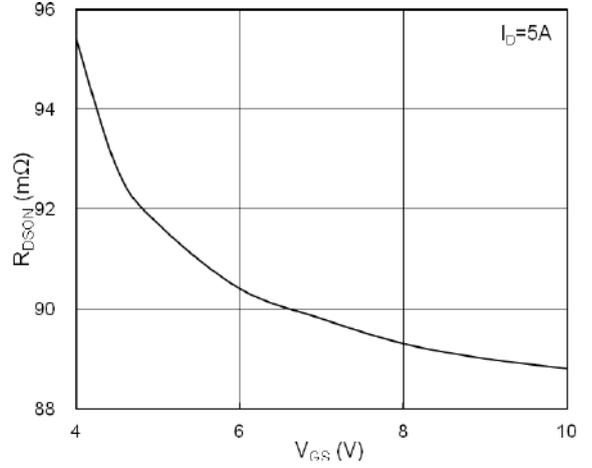
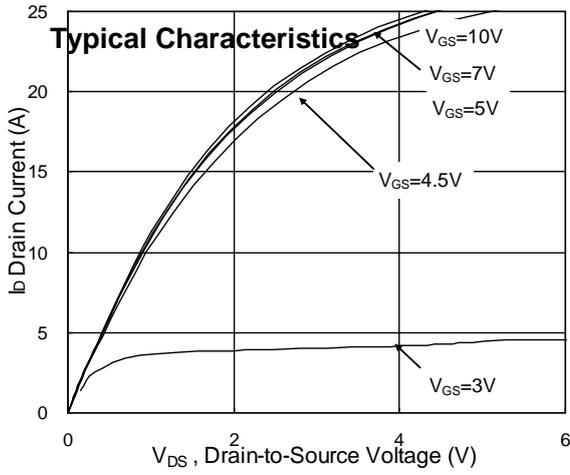


Fig.3 Forward Characteristics Of Reverse

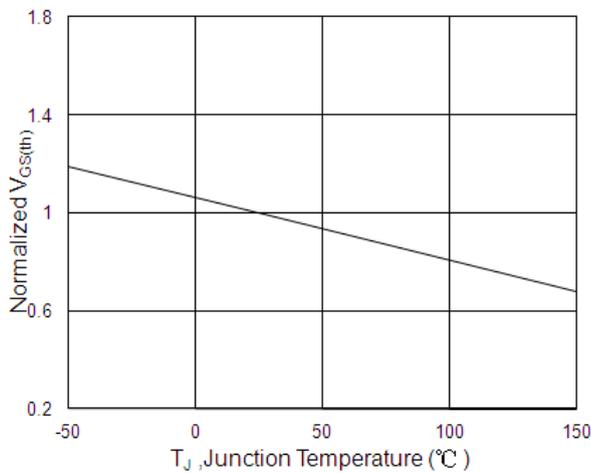


Fig.4 Gate-Charge Characteristics

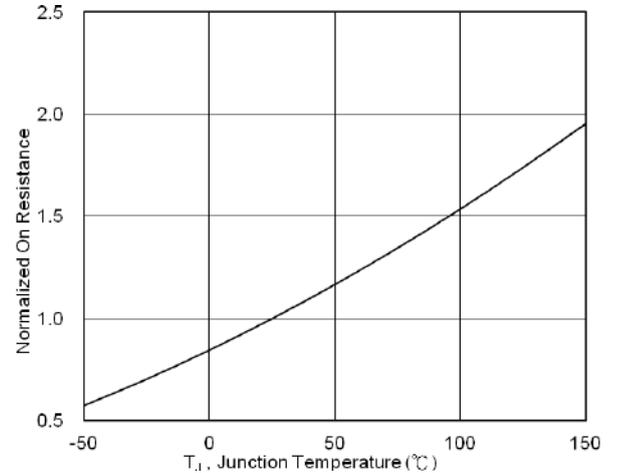


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J

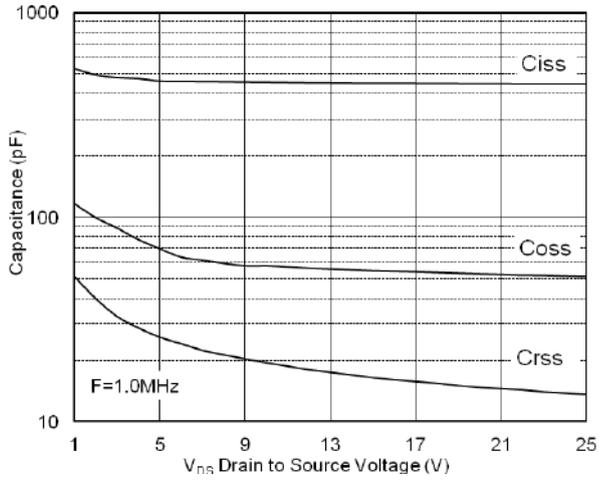


Fig.7 Capacitance

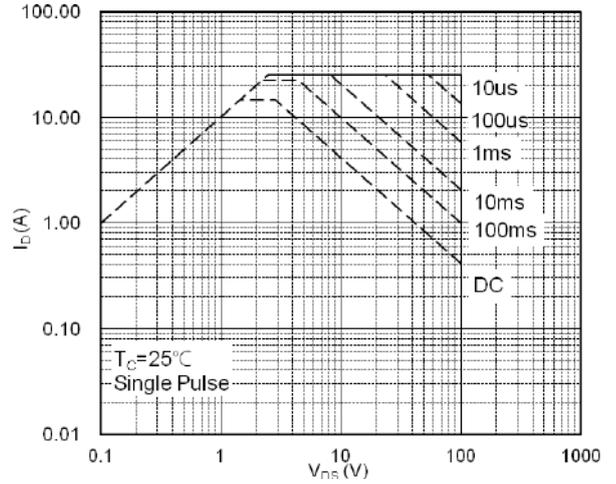
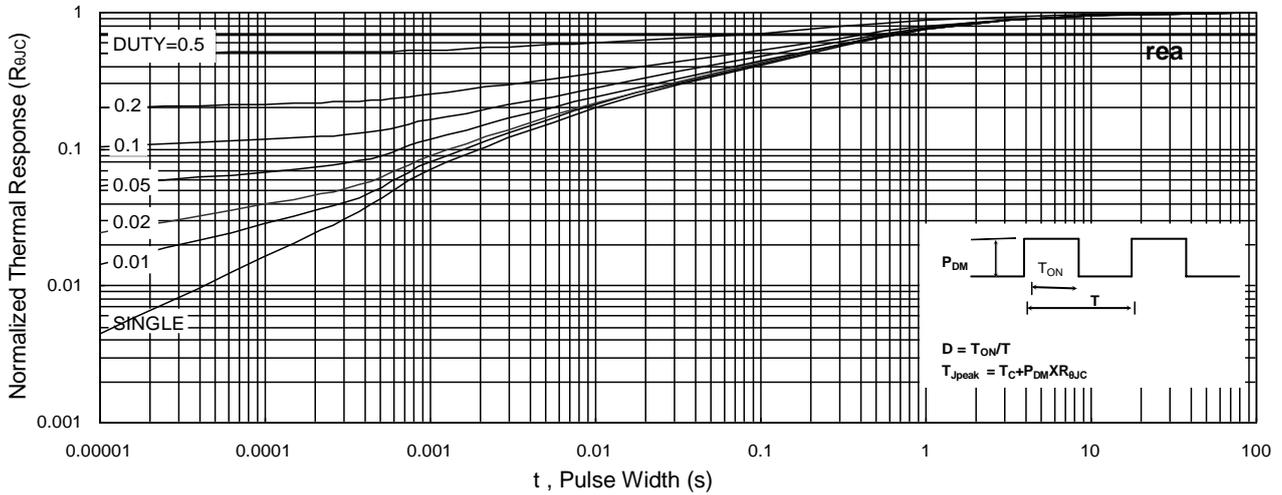


Fig.8 Safe Operating A



Normalized Maximum Transient Thermal Impedance

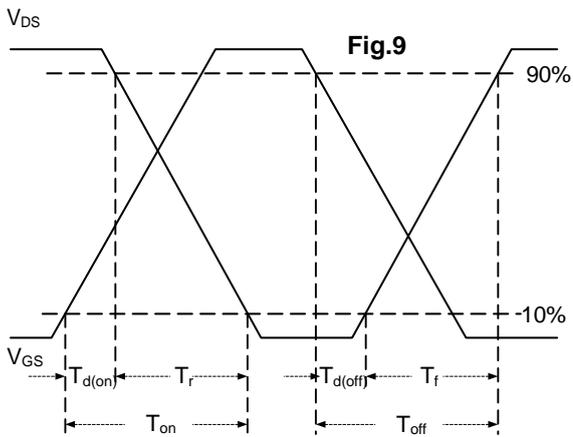


Fig.10 Switching Time Waveform

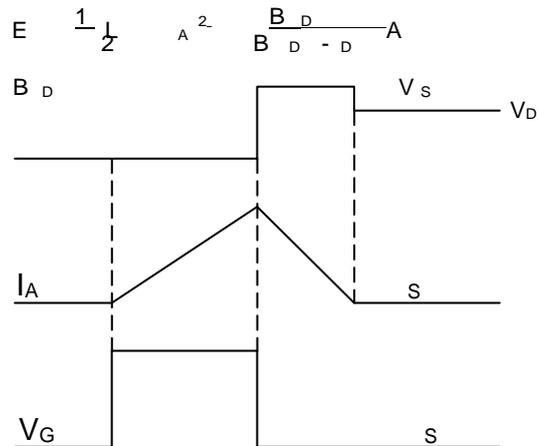


Fig.11 Unclamped Inductive Switching Waveform