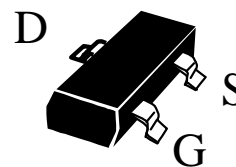


## P-Channel High Density Trench MOSFET

### Features:

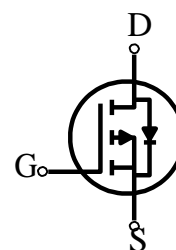
- Super high dense cell trench design for low RDS(on).
- Rugged and reliable.
- Surface Mount package.

SOT-23



### PRODUCT SUMMARY

VDSS	ID	RDS(on) (m-ohm)Max
-20V	-2.8	95 @ VGS= 4.5V
	-2.0	140 @ VGS= 2.5V



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	-20	V
Gate-Source Voltage	VGS	± 8	V
Drain Current-Continuous <sup>a</sup> @ T <sub>A</sub> = 25 °C -Pulse <sup>b</sup>	ID	-2.8	A
	IDM	-8	A
Drain-Source Diode Forward Current <sup>a</sup>	IS	-0.75	A
Maximum Power Dissipation <sup>a</sup>	PD	1.25	W
		0.75	
Operating Junction and Storage Temperature Range	TJ,TSTG	- 55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance,Junction-to-Ambient <sup>a</sup>	RthJA	100	°C/W
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Note

a. Surface Mounted on FR4 Board , t ≤ 10sec .

b. Pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V , I <sub>D</sub> = -250uA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -20V , V <sub>GS</sub> = 0V			-1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±8V , V <sub>DS</sub> = 0V			-100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250uA	-0.45	-0.65	-0.95	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5V , I <sub>D</sub> = -2.8A		75	95	m-ohm
		V <sub>GS</sub> = -2.5V , I <sub>D</sub> = -2.0A		90	140	m-ohm
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V , I <sub>S</sub> = -0.75A			-1.2	V
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -6V , V <sub>GS</sub> = 0V f = 1.0MHz		664		pF
Output Capacitance	C <sub>OSS</sub>			154		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			129		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = -6V , I <sub>D</sub> = -1A		8.6		ns
Rise Time	t <sub>r</sub>	V <sub>GEN</sub> = -4.5V		3.0		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>	R <sub>L</sub> = 6 ohm		39.2		ns
Fall Time	t <sub>f</sub>	R <sub>GEN</sub> = 6 ohm		11.2		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -6V I <sub>D</sub> = -2.8A V <sub>GS</sub> = -4.5V		6.72		nC
Gate-Source Charge	Q <sub>gs</sub>			1.12		nC
Gate-Drain Charge	Q <sub>gd</sub>			1.04		nC

Note

b. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2% .

c. Guaranteed by design , not subject to production testing .

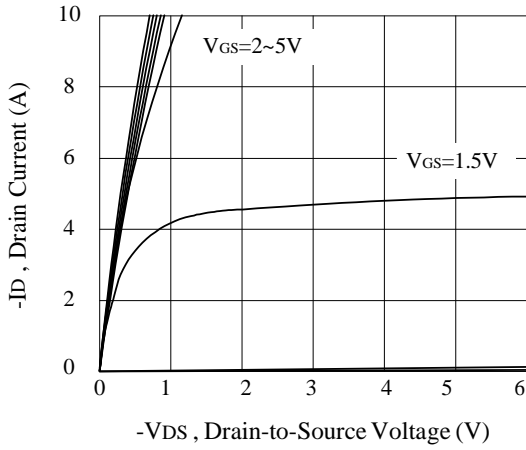


Figure 1. Output Characteristics

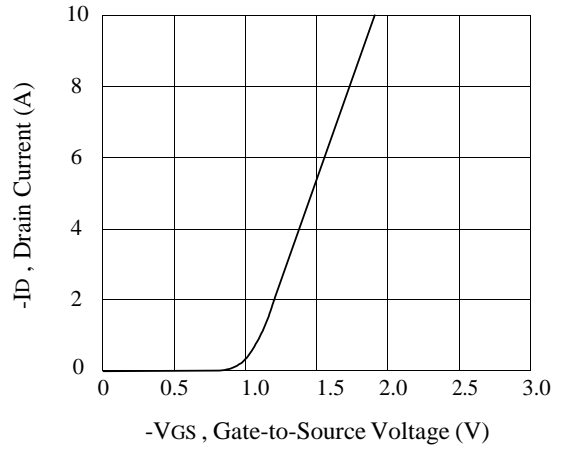


Figure 2. Transfer Characteristics

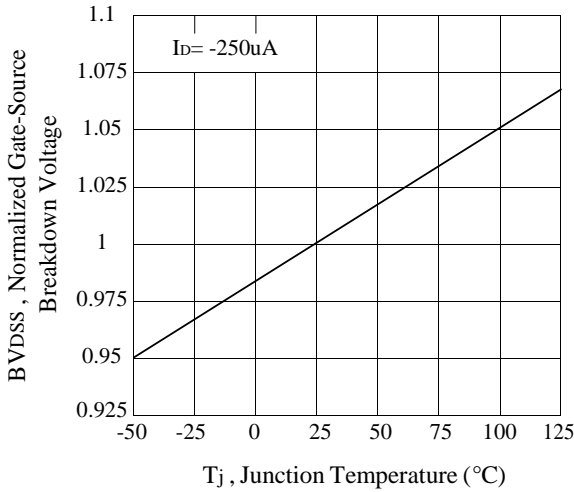


Figure 3. Breakdown Voltage Variation with Temperature

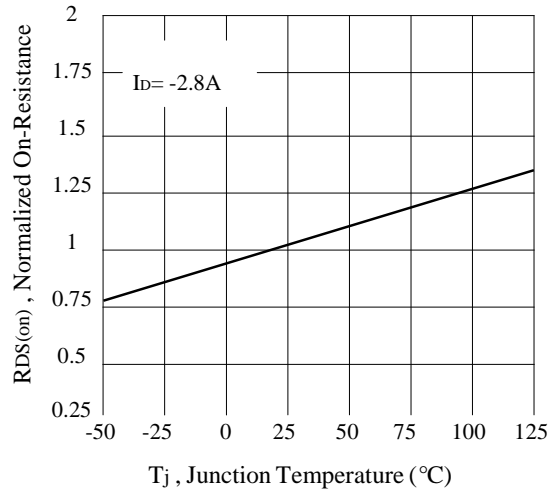


Figure 4. On-Resistance Variation with Temperature

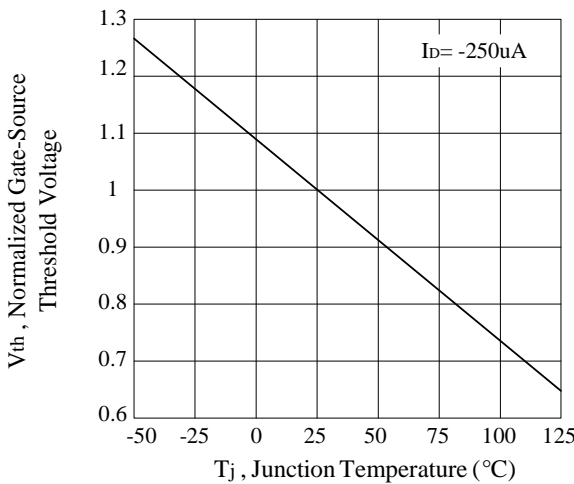


Figure 5. Gate Threshold Variation with Temperature

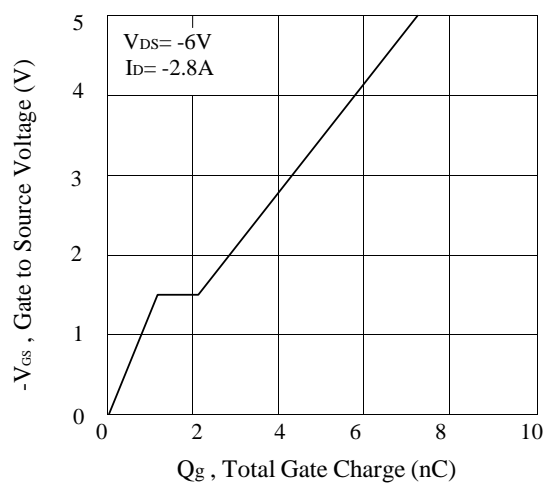
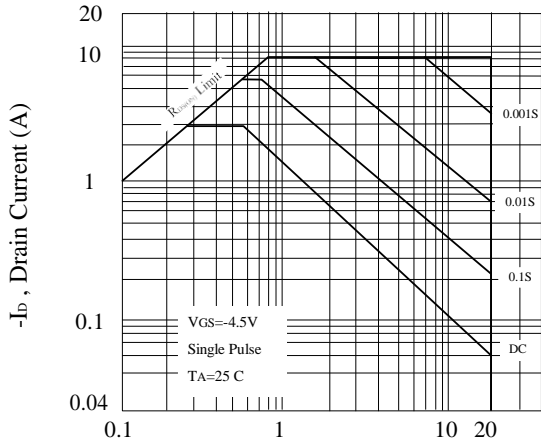
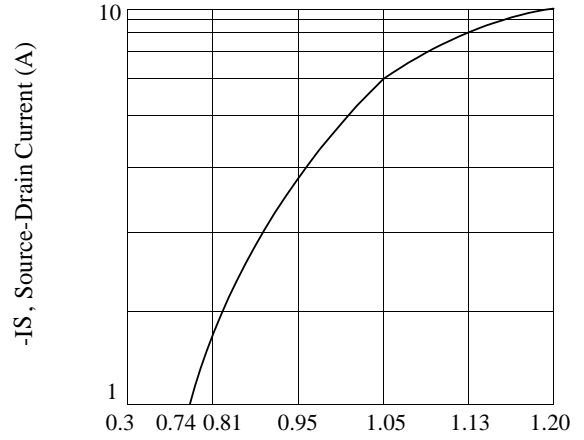


Figure 6. Gate Charge



-VDS, Drain-Source Voltage (V)  
 Figure 7. Maximum Safe Operating Area



-VSD, Body Diode Forward Voltage (V)  
 Figure 8. Body Diode Forward Voltage Variation with Source Current

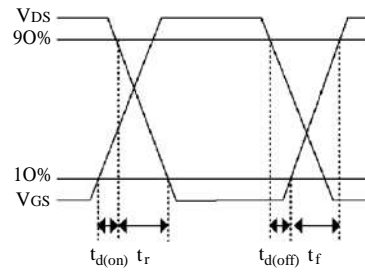
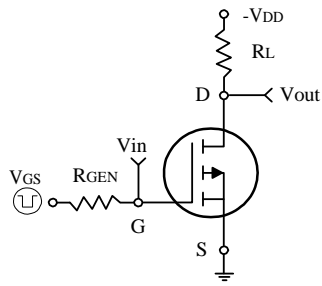


Figure 9. Switching Test Circuit and Switching Waveforms

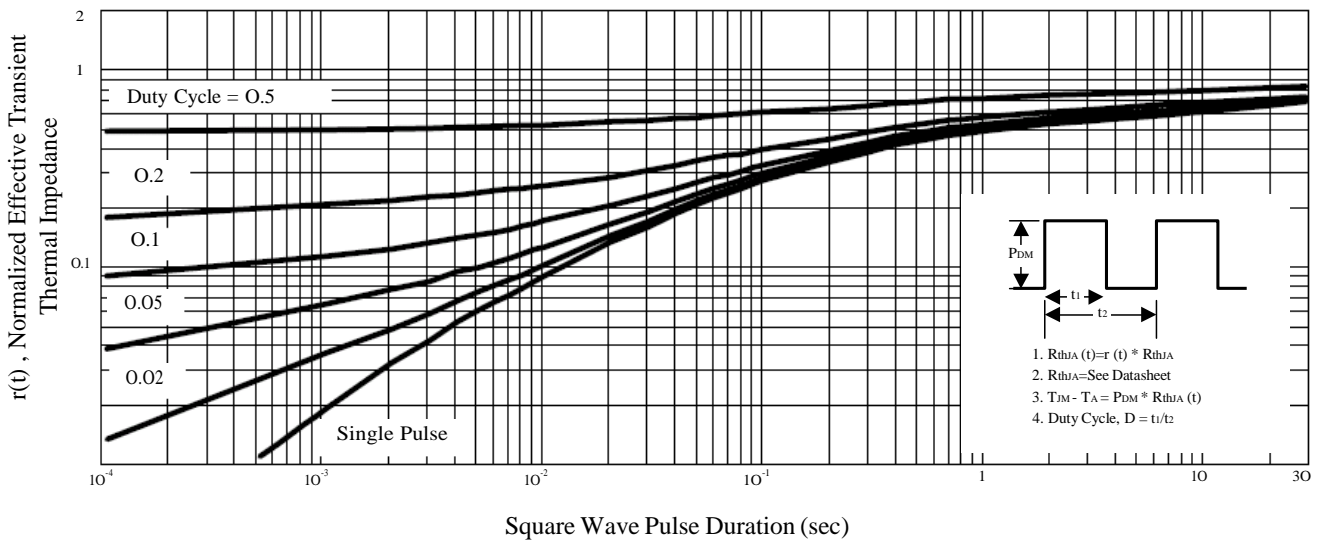


Figure 10. Normalized Thermal Transient Impedance Curve